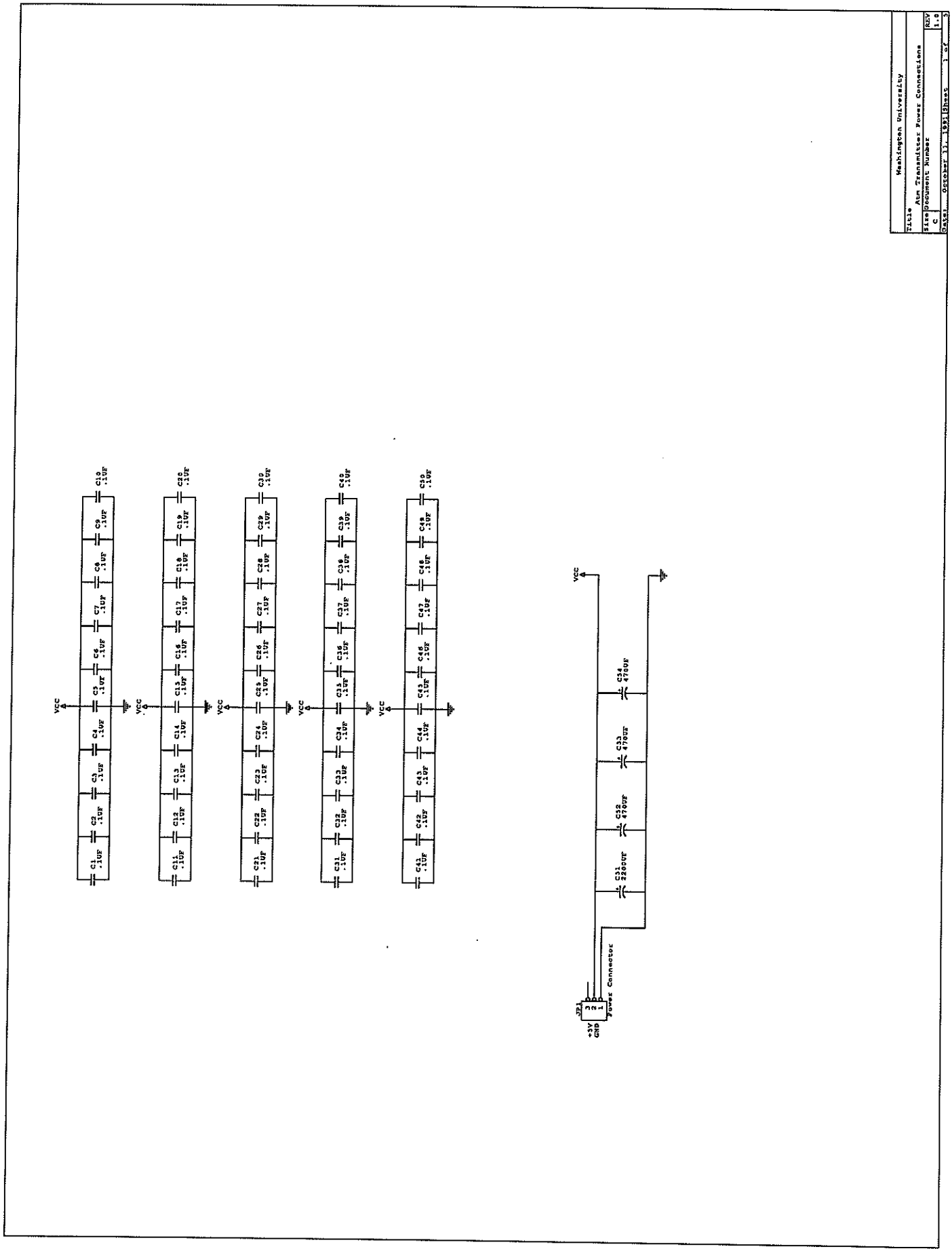
Appendix A

Mini-ATMizer Transmitter Schematics


Washington University
Title
Atm Transmitter Power Connections
Size
C
Document Number
REV
1.0
Date:
October 17, 1991
Sheet
1 of 1
VCC
+5V
GND
JP1
Power Connector
C1 .10UF
C2 .10UF
C3 .10UF
C4 .10UF
C5 .10UF
C6 .10UF
C7 .10UF
C8 .10UF
C9 .10UF
C10 .10UF
C11 .10UF
C12 .10UF
C13 .10UF
C14 .10UF
C15 .10UF
C16 .10UF
C17 .10UF
C18 .10UF
C19 .10UF
C20 .10UF
C21 .10UF
C22 .10UF
C23 .10UF
C24 .10UF
C25 .10UF
C26 .10UF
C27 .10UF
C28 .10UF
C29 .10UF
C30 .10UF
C31 .10UF
C32 .10UF
C33 .10UF
C34 .10UF
C35 .10UF
C36 .10UF
C37 .10UF
C38 .10UF
C39 .10UF
C40 .10UF
C41 .10UF
C42 .10UF
C43 .10UF
C44 .10UF
C45 .10UF
C46 .10UF
C47 .10UF
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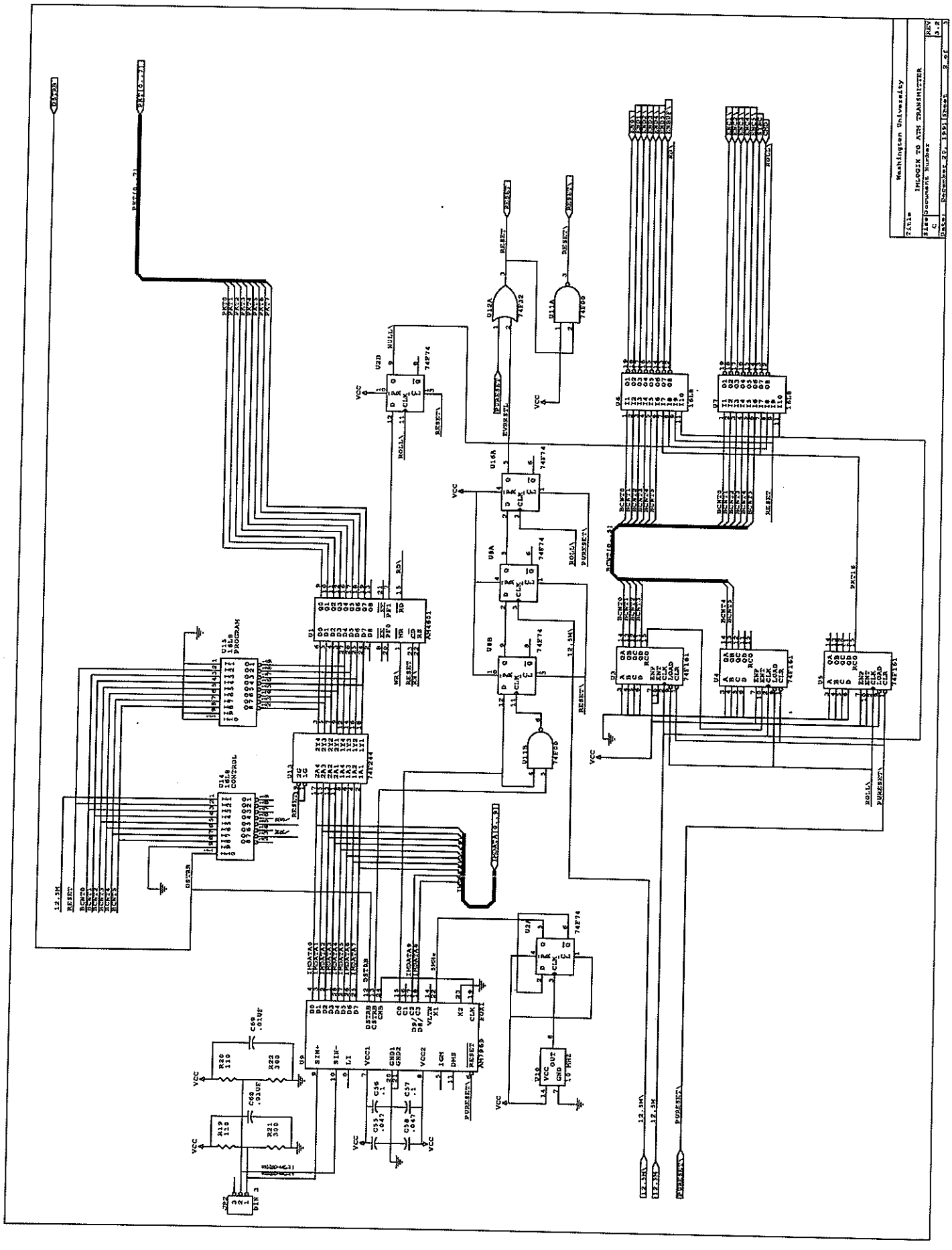
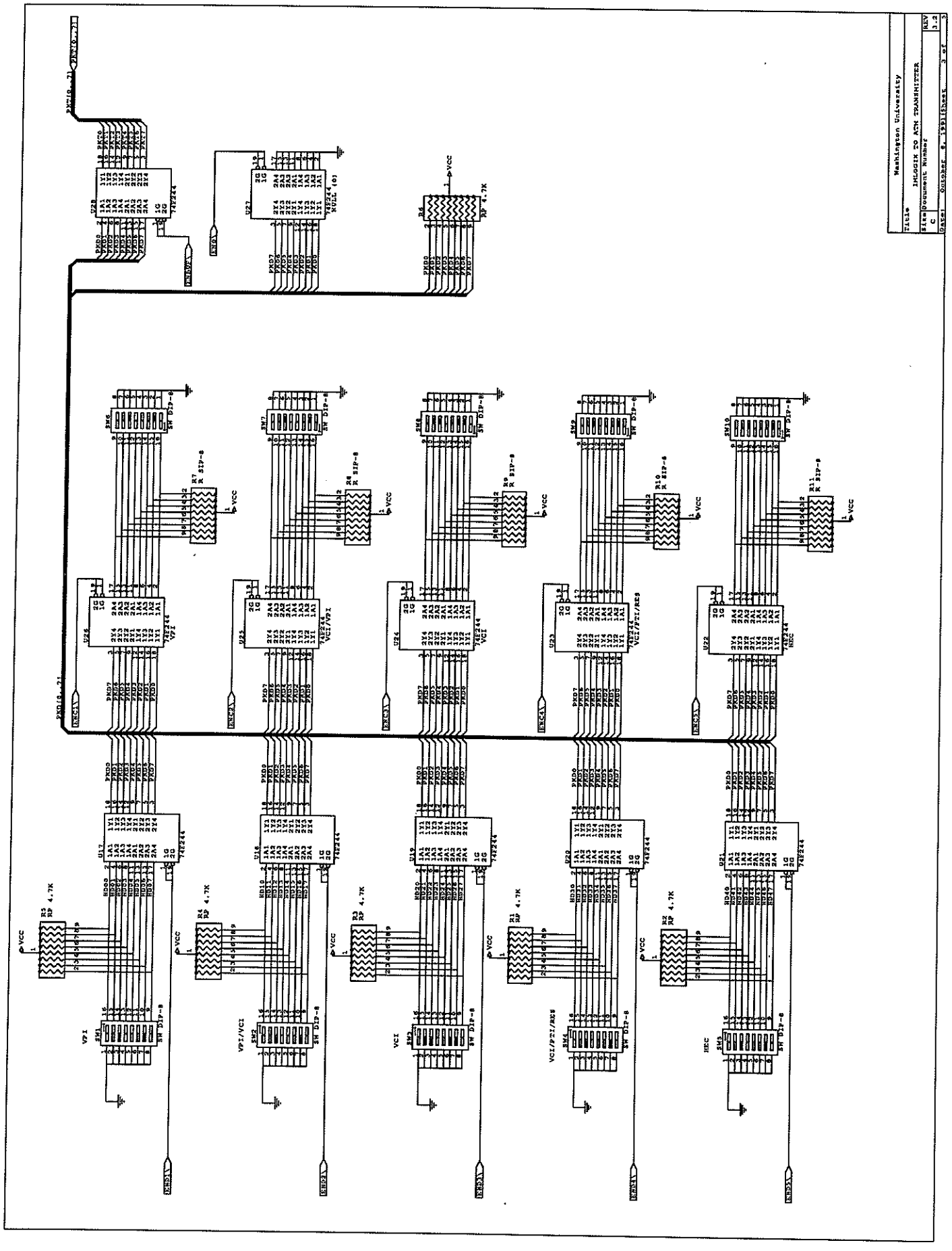
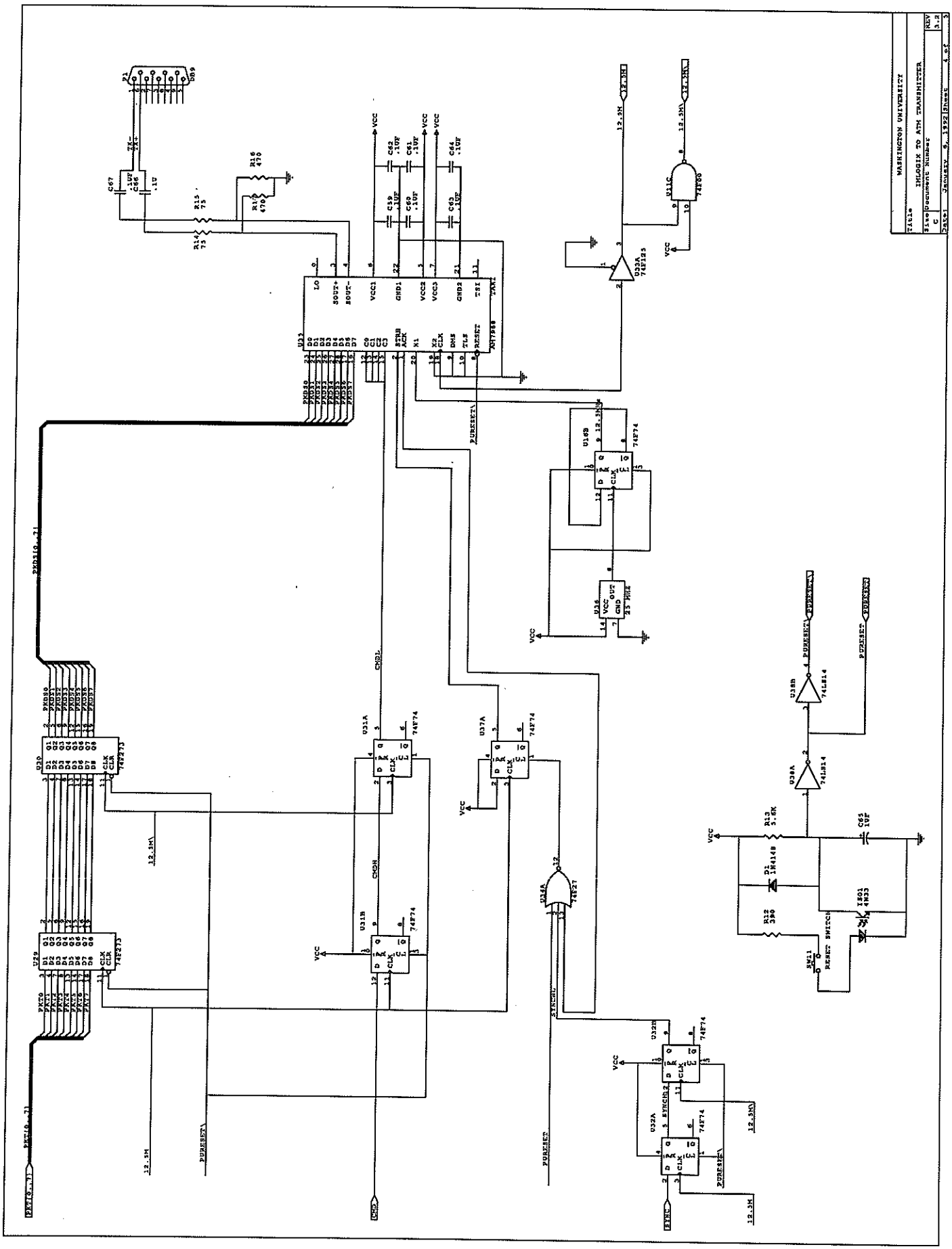
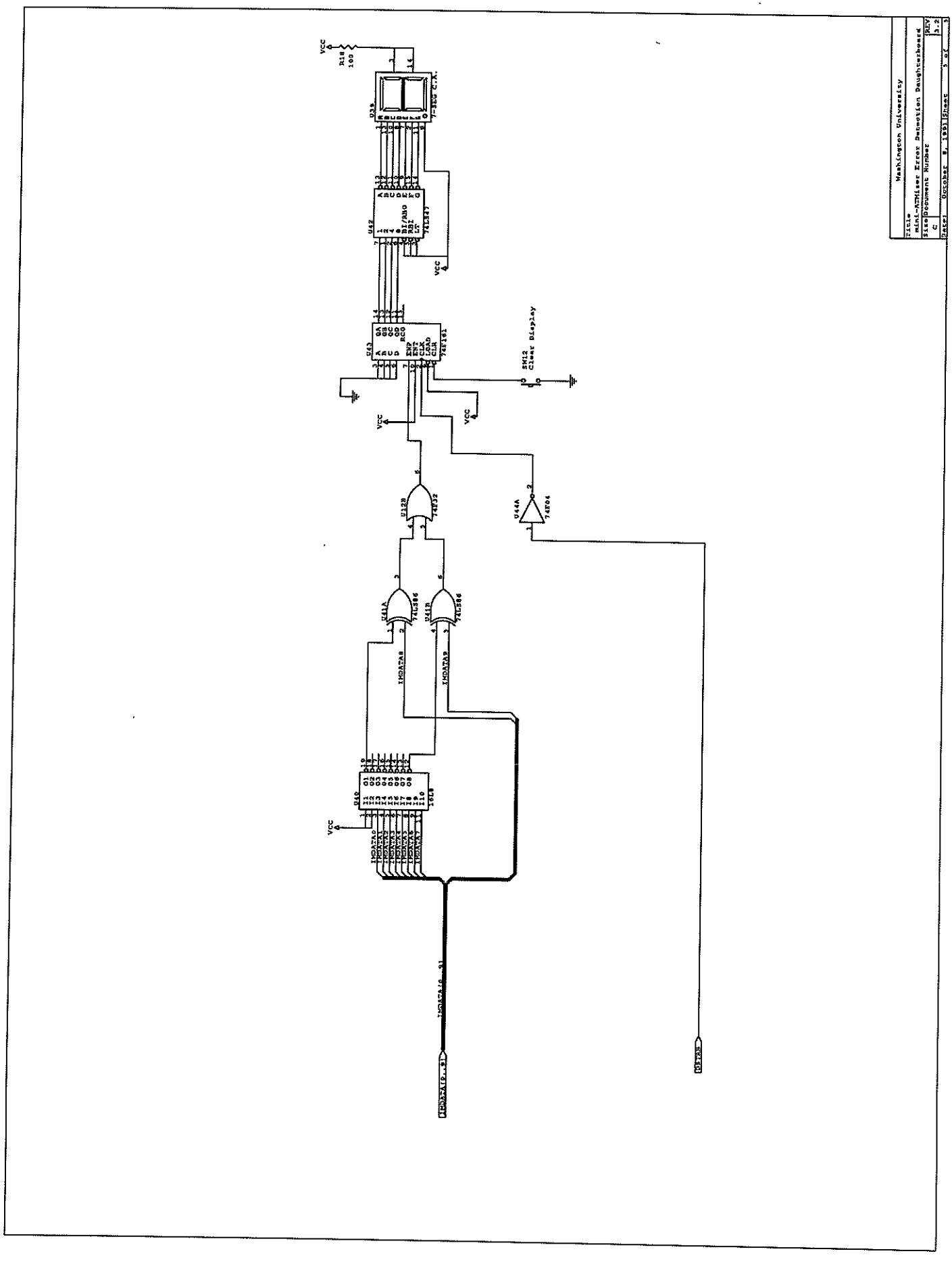
C49 .10UF
C50 .10UF
C31 2200UF
C32 470UF
C33 470UF
C34 470UF



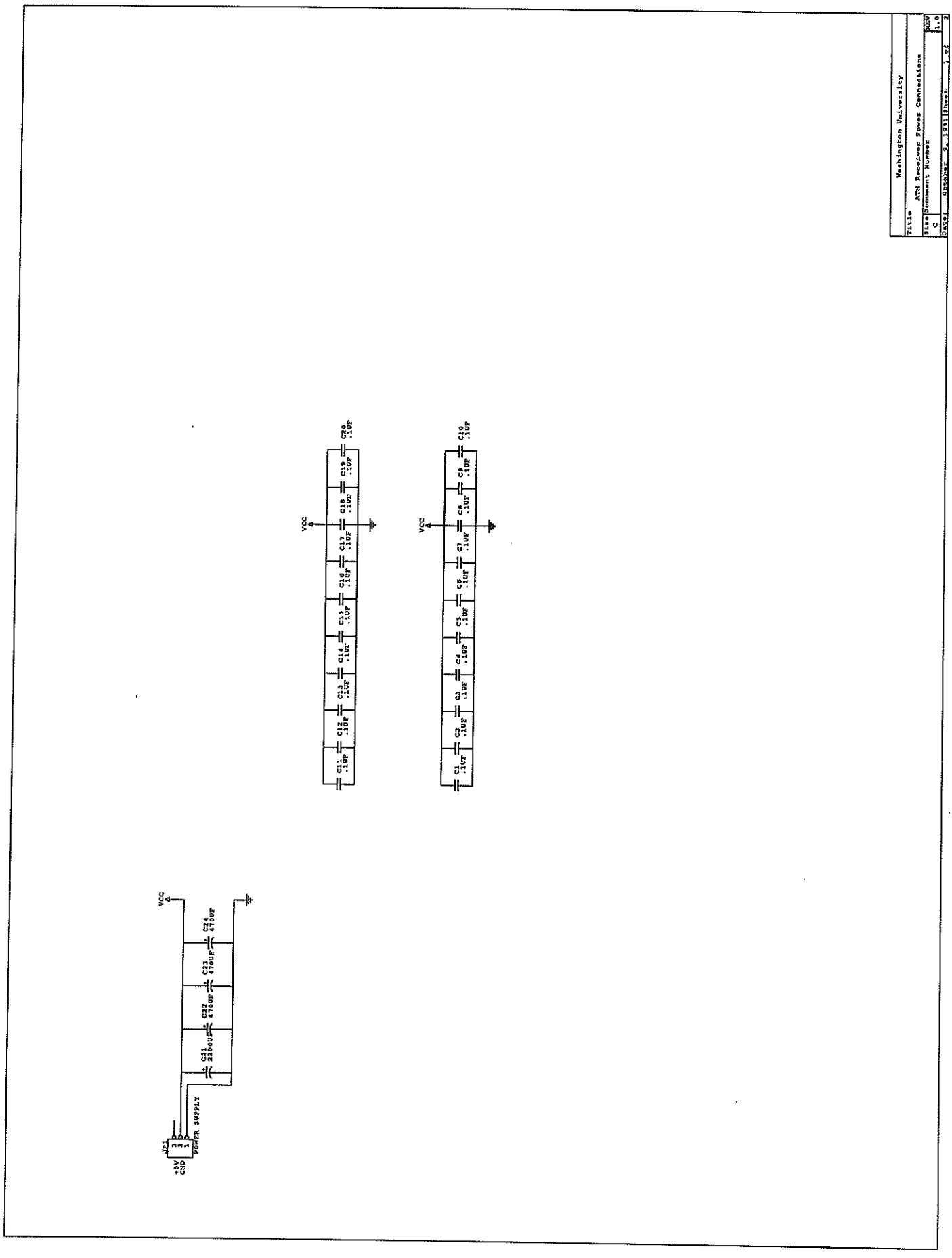

Washington University
Title
IMLOGIX 2G ATM TRANSMITTER
Size
Document Number
REV
3.2
C
Date: October 8, 1998
Sheet 3 of 4
VCC
VPI
VPI/VCI
VCI
VCI/PTI/RES
HEC

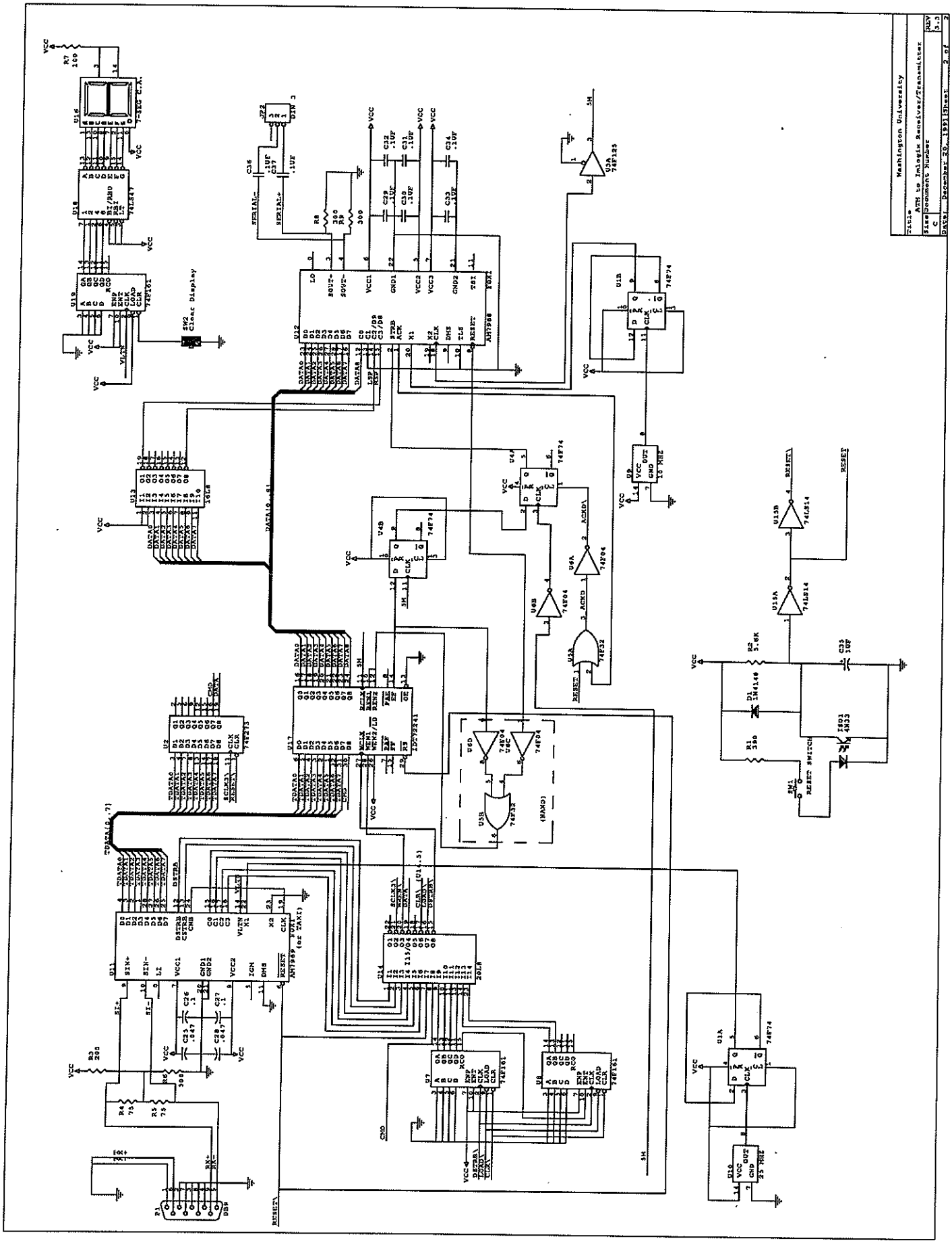



Washington University
Title
mini-ATMizer Error Detection Daughterboard
Size
C
Document Number
REV
3.0
Date:
October 8, 1993
Sheet
3 of 3
VCC
R18
100
U39
U42
U43
SW12
Clear Display
U41A
U41B
U44A
74F04
74F32
74C86
IMDATA0
IMDATA1
IMDATA2
IMDATA3
IMDATA4
IMDATA5
IMDATA6
IMDATA7
IMDATA[7..0]
DETECT

Appendix B

Mini-ATMizer Receiver Schematics


Washington University
Title
ATM Receiver Power Connections
Size
C
Document Number
Rev
1.0
Date: October 9, 1991
Sheet
1 of 2
VCC
C1 .1UF
C2 .1UF
C3 .1UF
C4 .1UF
C5 .1UF
C6 .1UF
C7 .1UF
C8 .1UF
C9 .1UF
C10 .1UF
C11 .1UF
C12 .1UF
C13 .1UF
C14 .1UF
C15 .1UF
C16 .1UF
C17 .1UF
C18 .1UF
C19 .1UF
C20 .1UF
C21 2200uF
C22 470uF
C23 470uF
C24 470uF
JP1
+5V
GND
POWER SUPPLY


Washington University
Title
ATM to Integrix Receiver/Transmitter
Size
C
Document Number
REV
3.3
Date: December 20, 1995
Sheet 2 of 2

Appendix C

PAL Equations

```
TITLE       Transmitter Control PAL 1 (U6)
PATTERN     txtrcon1.pds
REVISION    2
AUTHOR      David M. Zar
COMPANY     Washington University (ERL)
DATE        Aug. 8, 1991

CHIP        tctrcon1    PAL16L8

BCNT0   BCNT1   BCNT2   BCNT3   BCNT4   BCNT5   PKT16   /NULL   RESET   GND
M12     /ENR    /ENBUF  /END5   /END4   /END3   /END2   /END1   /EN0    VCC

EQUATIONS

EN0     = NULL*/M12*/RESET
        + RESET*/M12*BCNT5
        + RESET*/M12*/BCNT5*BCNT4
        + RESET*/M12*/BCNT5*/BCNT4*BCNT3
        + RESET*/M12*/BCNT5*/BCNT4*/BCNT3*BCNT2*BCNT1
        + RESET*/M12*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*BCNT0

END1    = /RESET*/NULL*/BCNT5*/BCNT4*/BCNT3*/BCNT2*/BCNT1*/BCNT0*/M12
END2    = /RESET*/NULL*/BCNT5*/BCNT4*/BCNT3*/BCNT2*/BCNT1*BCNT0*/M12
END3    = /RESET*/NULL*/BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1*/BCNT0*/M12
END4    = /RESET*/NULL*/BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1*BCNT0*/M12
END5    = /RESET*/NULL*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0*/M12

ENBUF   = NULL*/M12*/RESET
        + /M12*/BCNT5*/BCNT4*/BCNT3*/BCNT2
        + /M12*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0

ENR     = /RESET*/NULL*/M12*BCNT5*BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0
        + /RESET*/NULL*/M12*BCNT5*BCNT4*/BCNT3*/BCNT2
        + /RESET*/NULL*/M12*BCNT5*/BCNT4
        + /RESET*/NULL*/M12*/BCNT5*BCNT4
        + /RESET*/NULL*/M12*/BCNT5*/BCNT4*BCNT3
        + /RESET*/NULL*/M12*/BCNT5*/BCNT4*/BCNT3*BCNT2*BCNT1
        + /RESET*/NULL*/M12*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*BCNT0


SIMULATION

SETF /RESET /NULL /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12

SETF RESET /NULL /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
```

```
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12

SETF /RESET NULL /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
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SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12

SETF RESET NULL /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
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SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
```

```
TITLE       Transmitter Control PAL 2 (U7)
PATTERN     txtrcon2.pds
REVISION    1
AUTHOR      David M. Zar
COMPANY     Washington University (ERL)
DATE        Aug. 8, 1991

CHIP        tctrcon1    PAL16L8

BCNT0   BCNT1   BCNT2   BCNT3   BCNT4   BCNT5   PKT16   /NULL   RESET   GND
M12     /ROLL   CMD     SYNC    /ENC5   /ENC4   /ENC3   /ENC2   /ENC1    VCC

EQUATIONS

ENC1    = RESET*/BCNT5*/BCNT4*/BCNT3*/BCNT2*/BCNT1*/BCNT0*/M12
ENC2    = RESET*/BCNT5*/BCNT4*/BCNT3*/BCNT2*/BCNT1*BCNT0*/M12
ENC3    = RESET*/BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1*/BCNT0*/M12
ENC4    = RESET*/BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1*BCNT0*/M12
ENC5    = RESET*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0*/M12

ROLL    = /PKT16*/M12*BCNT5*BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0
        + PKT16 */M12*BCNT5*BCNT4*/BCNT3*BCNT2*BCNT1*/BCNT0

CMD     = /M12*BCNT5*BCNT4*/BCNT3*BCNT2*BCNT1*/BCNT0

SYNC    = /M12*BCNT5*BCNT4*/BCNT3*BCNT2*/BCNT1*BCNT0

SIMULATION

SETF /PKT16 /RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
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SETF /M12
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SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
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SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12

SETF /PKT16 RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12
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SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
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SETF /M12
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SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
```

```
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /BCNT5 /BCNT4 BCNT3 /BCNT2 BCNT1 /BCNT0 M12
SETF /M12

SETF /PKT16 BCNT5 BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF BCNT5 BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12

SETF PKT16 BCNT5 BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12
SETF /M12
SETF BCNT5 BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12
SETF /M12

SETF BCNT5 BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12
SETF /M12
SETF BCNT5 BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12
SETF /M12
SETF /PKT16 /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12
SETF /M12
```

```
TITLE           FIFO Control (U15)
PATTERN         FIFOCONT.PDS
REVISION        1
AUTHOR          David M. Zar
COMPANY         Washington University(ERL)
DATE            Aug. 8, 1991

CHIP    FIFOCont PAL16L8

M12     RESET   BCNT0   BCNT1   BCNT2   BCNT3   BCNT4   BCNT5   /ENR    GND
DSTRB   /RD     /WR     NC      /RS     NC      NC      NC      NC      VCC

EQUATIONS

RD      = /RESET*ENR
RD.TRST = VCC

RS      = RESET*/M12*/BCNT5*/BCNT4*/BCNT3*/BCNT2*/BCNT1*/BCNT0
RS.TRST = VCC

WR      = DSTRB
        + /M12*RESET*/BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1
        + /M12*RESET*/BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1
WR.TRST = VCC

SIMULATION

TRACE_ON M12 RESET BCNT0 BCNT1 BCNT2 BCNT3 BCNT4 BCNT5 /WR /RD /RS

SETF    /DSTRB
SETF    RESET BCNT5 BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0 /M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 M12

SETF    RESET /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0 /M12

TRACE_OFF
```

```
TITLE           FIFO Programming Data Generator (U14)
PATTERN         PROGDATA.PDS
REVISION        1
AUTHOR          David M. Zar
COMPANY         Washington University(ERL)
DATE            Aug. 8, 1991

CHIP    progdata PAL16L8

NC      RESET   BCNT0   BCNT1   BCNT2   BCNT3   BCNT4   BCNT5   NC      GND
NC      /D0     /D1     /D2     /D3     /D7     /D6     /D5     /D4     VCC

EQUATIONS

D0      = VCC
D0.TRST = RESET

D1      = VCC
D1.TRST = RESET

D2      = VCC
D2.TRST = RESET

D3      = VCC
D3.TRST = RESET

D4      = GND
D4.TRST = RESET

D5      = /BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*BCNT0
D5.TRST = RESET

D6      = /BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0
D6.TRST = RESET

D7      = /BCNT5*/BCNT4*/BCNT3*/BCNT2*BCNT1*BCNT0
        + /BCNT5*/BCNT4*/BCNT3*BCNT2*/BCNT1*/BCNT0
D7.TRST = RESET

SIMULATION

SETF /RESET
SETF BCNT5 BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0
SETF RESET
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0
SETF /RESET
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 BCNT2 BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 /BCNT1 BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 /BCNT0
SETF /BCNT5 /BCNT4 /BCNT3 /BCNT2 BCNT1 BCNT0
```

```
TITLE           modular 4 parity generator for ATM to Imlogix box (U13)
PATTERN         parity.pds
REVISION        1
AUTHOR          Greg Hassen (David Zar)
COMPANY         Washington University (ERL)
DATE            Aug 8, 1991

CHIP parity PAL16L8

/LSB    /MSB    DIN0    DIN1    DIN2    DIN3    DIN4    DIN5    DIN6    GND
DIN7    /LSB4   /MSB3   /LSB3   /MSB2   /LSB2   /MSB1   /LSB1   /MSB4   VCC

EQUATIONS

LSB1    = /LSB*/MSB*DIN0*/DIN1
        + /LSB*/MSB*DIN0*DIN1
        + /LSB*MSB*DIN0*/DIN1
        + /LSB*MSB*DIN0*DIN1
        + LSB*/MSB*/DIN0*/DIN1
        + LSB*/MSB*/DIN0*DIN1
        + LSB*MSB*/DIN0*/DIN1
        + LSB*MSB*/DIN0*DIN1

MSB1    = /LSB*/MSB*/DIN0*DIN1
        + /LSB*/MSB*DIN0*DIN1
        + /LSB*MSB*/DIN0*/DIN1
        + /LSB*MSB*DIN0*/DIN1
        + LSB*/MSB*/DIN0*DIN1
        + LSB*/MSB*DIN0*DIN1
        + LSB*MSB*/DIN0*/DIN1
        + LSB*MSB*DIN0*/DIN1

LSB2    = /LSB1*/MSB1*DIN2*/DIN3
        + /LSB1*/MSB1*DIN2*DIN3
        + /LSB1*MSB1*DIN2*/DIN3
        + /LSB1*MSB1*DIN2*DIN3
        + LSB1*/MSB1*/DIN2*/DIN3
        + LSB1*/MSB1*/DIN2*DIN3
        + LSB1*MSB1*/DIN2*/DIN3
        + LSB1*MSB1*/DIN2*DIN3

MSB2    = /LSB1*/MSB1*/DIN2*DIN3
        + /LSB1*/MSB1*DIN2*DIN3
        + /LSB1*MSB1*/DIN2*/DIN3
        + /LSB1*MSB1*DIN2*/DIN3
        + LSB1*/MSB1*/DIN2*DIN3
        + LSB1*/MSB1*DIN2*DIN3
        + LSB1*MSB1*/DIN2*/DIN3
        + LSB1*MSB1*DIN2*/DIN3

LSB3    = /LSB2*/MSB2*DIN4*/DIN5
        + /LSB2*/MSB2*DIN4*DIN5
        + /LSB2*MSB2*DIN4*/DIN5
        + /LSB2*MSB2*DIN4*DIN5
        + LSB2*/MSB2*/DIN4*/DIN5
        + LSB2*/MSB2*/DIN4*DIN5
        + LSB2*MSB2*/DIN4*/DIN5
        + LSB2*MSB2*/DIN4*DIN5

MSB3    = /LSB2*/MSB2*/DIN4*DIN5
        + /LSB2*/MSB2*DIN4*DIN5
        + /LSB2*MSB2*/DIN4*/DIN5
        + /LSB2*MSB2*DIN4*/DIN5
        + LSB2*/MSB2*/DIN4*DIN5
        + LSB2*/MSB2*DIN4*DIN5
        + LSB2*MSB2*/DIN4*/DIN5
        + LSB2*MSB2*DIN4*/DIN5
```

```
LSB4    = /LSB3*/MSB3*DIN6*/DIN7
        + /LSB3*/MSB3*DIN6*DIN7
        + /LSB3*MSB3*DIN6*/DIN7
        + /LSB3*MSB3*DIN6*DIN7
        + LSB3*/MSB3*/DIN6*/DIN7
        + LSB3*/MSB3*/DIN6*DIN7
        + LSB3*MSB3*/DIN6*/DIN7
        + LSB3*MSB3*/DIN6*DIN7

MSB4    = /LSB3*/MSB3*/DIN6*DIN7
        + /LSB3*/MSB3*DIN6*DIN7
        + /LSB3*MSB3*/DIN6*/DIN7
        + /LSB3*MSB3*DIN6*/DIN7
        + LSB3*/MSB3*/DIN6*DIN7
        + LSB3*/MSB3*DIN6*DIN7
        + LSB3*MSB3*/DIN6*/DIN7
        + LSB3*MSB3*DIN6*/DIN7
```

```
TITLE       Receiver Control PAL (U14)
PATTERN     rcvcont.pds
REVISION    2
AUTHOR      David M. Zar
COMPANY     Washington University (ERL)
DATE        Aug. 8, 1991

CHIP        rcvcont PAL20L8

;1      2       3   4   5   6   7       8   9   10  11  12
DSTRB   CSTRB   CD0 CD1 CD2 CD3 /RESET  CMD C0  C1  C2  GND

;13 14  15      16      17      18      19      20      21      22  23  24
C3  C4  /DSTRBO /LOAD   /CLR    /TSTCLK DATA    /WREN   /SCLK3  NC  C5  VCC

EQUATIONS

DSTRBO  = DSTRB*/RESET

CLR     = RESET
        + CSTRB*CD0*CD1*CD2*CD3

LOAD    = C5*C4*/C3*C2*/C1*/C0*/RESET

SCLK3   = /C5*/C4*/C3*/C2*C1*C0*/RESET*DSTRB

WREN    = C5*DATA*/CMD
        + /C5*C4*DATA*/CMD
        + /C5*/C4*C3*DATA*/CMD
        + /C5*/C4*/C3*C2*C1*DATA*/CMD
        + /C5*/C4*/C3*C2*/C1*C0*DATA*/CMD
        + /C5*/C4*/C3*C2*/C1*C0*/DATA*CMD

TSTCLK  = DSTRB*C5*DATA*/CMD
        + DSTRB*/C5*C4*DATA*/CMD
        + DSTRB*/C5*/C4*C3*DATA*/CMD
        + DSTRB*/C5*/C4*/C3*C2*C1*DATA*/CMD
        + DSTRB*/C5*/C4*/C3*C2*/C1*C0*DATA*/CMD
        + DSTRB*/C5*/C4*/C3*C2*/C1*C0*/DATA*CMD

SIMULATION

TRACE_ON C5 C4 C3 C2 C1 C0 /WREN /SCLK3 /LOAD DATA

SETF /RESET
SETF /C5 /C4 /C3 /C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 /C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 DATA /CMD /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 C3 /C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 C3 /C2 /C1 C0 /DSTRB

SETF RESET DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DSTRB /DATA CMD
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 C0 /DSTRB
```

```
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DSTRB

SETF /RESET DSTRB
SETF /C5 /C4 /C3 /C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 /C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DATA CMD /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 C2 C1 C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 C3 /C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 C3 /C2 /C1 C0 /DSTRB

SETF C5 C4 /C3 /C2 C1 /C0 /DSTRB
SETF DSTRB
SETF C5 C4 /C3 /C2 C1 C0 /DSTRB
SETF DSTRB
SETF C5 C4 /C3 C2 /C1 /C0 /DSTRB
SETF DSTRB
SETF /C5 /C4 /C3 /C2 /C1 /C0 /DSTRB
SETF DSTRB

TRACE_OFF
```

Appendix D

Mini-ATMizer Parts Lists

Atm Transmitter Parts List — Revised: October 11, 1991
Revision: 1.0 Bill Of Materials — November 18, 1991 9:19:54

Item	Quantity	Reference	Part	DESCRIPTION	PART ORDER #
1	1	D1	1N4148	Diode	
2	1	ISO1	4N33	Opto-Isolator	
3	1	P1	DB9	DB9 Male PC Board Connector	
4	1	SW11	RESET SWITCH	SPST Momentary Push-Button Switch	
5	1	SW12	Clear Display	SPST Momentary Push-Button Switch	
6	6	U2,U8,U16,U31,U32,U37	74F74	Dual D-Type Flip-Flop with Preset and Clear	
7	2	U29,U30	74F273	Octal D-Type Flip-Flops	
8	1	U33	74F125	Quad Buffer Tri-State Gates	
9	1	U12	74F32	Quad 2-Input OR Gates	
10	1	U44	74F04	Hex Inverters	
11	4	U3,U4,U5,U43	74F161	Synchronous 4-bit Binary Counters	
12	1	U10	10 MHZ	10 MHz (.01%) Oscillator	
13	1	U36	25 MHZ	25 MHz (.01%) Oscillator	
14	1	U9	AM7969	TAXI Receiver - (FOXI in real life)	
15	1	U35	AM7968	TAXI Transmitter - (FOXI in real life)	
16	5	U6,U7,U14,U15,U40	16L8	16L8 5ns PAL	TIBPAL16L8-5
17	1	U38	74LS14	Hex Schmitt-Trigger Inverters	
18	1	U39	7-SEG C.A.	7-Segment Common Annode Display	
19	6	R1,R2,R3,R4,R5,R6	RP 4.7K	4.7K Resistor SIPS	
20	5	R7,R8,R9,R10,R11	R SIP-8	4.7K Resistor SIPS	
21	10	SW1,SW2,SW3,SW4,SW5,SW6, SW7,SW8,SW9,SW10	SW DIP-8	8-Position DIP Switch	
22	1	U1	AM4601	512x9 bit FIFO with Programmable Flags	AM4601-25RC
23	1	U41	74LS86	Quad 2-Input XOR Gates	
24	1	U42	74LS47	BCD to 7-Segment Display Driver	
25	1	U11	74F00	Quad 2-Input NAND Gates	
26	13	U13,U17,U18,U19,U20,U21, U22,U23,U24,U25,U26,U27, U28	74F244	Octal Buffers/Line Drivers	
27	1	U34	74F27	Triple 3-Input NOR Gates	
28	1	JP1	Power Connector	Three Pin Power Connector (+5V & Ground)	
29	57	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32, C33,C34,C35,C36,C37,C38, C39,C40,C41,C42,C43,C44, C45,C46,C47,C48,C49,C50, C59,C60,C61,C62,C63,C64, C67	.1UF	.1UF Decoupling Capacitor	
30	3	C52,C53,C54	470UF	470UF Electolytic	DigiKey P6230
31	1	C51	2200UF	2200UF Electolytic	DigiKey P6232
32	1	R12	390	390 Ohm 1/4 Watt Resistor	
33	1	R13	5.6K	5.6K Ohm 1/4 Watt Resistor	
34	2	R14,R15	75	75 Ohm 1/4 Watt Resistor	
35	2	R16,R17	470	470 Ohm 1/4 Watt Resistor	
36	1	R18	100	100 Ohm 1/4 Watt Resistor	
37	2	R19,R20	110	110 Ohm 1/4 Watt Resistor	
38	2	R21,R22	300	300 Ohm 1/4 Watt Resistor	
39	1	JP2	DIN 3	3 Pin Sub-mini DIN Connector	
40	2	C55,C58	.047	.047UF Ceramic Disc Capacitor	
41	2	C56,C57	.1	.1UF Ceramic Disc Capacitor	
42	1	C65	1UF	1UF Ceramic Disc Capacitor	
43	1	C66	.1U	.1UF Ceramic Disc Capacitor	
44	2	C68,C69	.01UF	.01UF Ceramic Disc Capacitor	

ATM Receiver Parts List
Revision: 1.0 Bill Of Materials
Revised: October 9, 1991
November 18, 1991 9:21:10

Item	Quantity	Reference	Part	DESCRIPTION	PART ORDER #
1	1	D1	1N4148	Diode	
2	1	ISO1	4N33	Opto-Isolator	
3	1	P1	DB9	DB9 Male PC Board Connector	
4	1	SW1	RESET SWITCH	SPST Momentary Push-Button Switch	
5	1	SW2	Clear Display	SPST Momentary Push-Button Switch	
6	2	U1,U4	74F74	Dual D-Type Flip-Flop with Preset and Clear	
7	1	U2	74F273	Octal D-Type Flip-Flops	
8	1	U3	74F125	Quad Buffer Tri-State Gates	
9	1	U5	74F32	Quad 2-Input OR Gates	
10	1	U6	74F04	Hex Inverters	
11	3	U7,U8,U19	74F161	Synchronous 4-bit Binary Counters	
12	1	U9	10 MHZ	10 MHz (.01%) Oscillator	
13	1	U10	25 MHZ	25 MHz (.01%) Oscillator	
14	1	U11	AM7969	TAXI Receiver - (FOXI in real life)	
15	1	U12	AM7968	TAXI Transmitter - (FOXI in real life)	
16	1	U13	16L8	16L8 5ns PAL	TIBIPAL16L8-5
17	1	U14	20L8	20L8 5ns PAL	TIBIPAL20L8-5
18	1	U15	74LS14	Hex Schmitt-Trigger Inverters	
19	1	U18	74LS47	BCD to 7-Segment Decoder	
20	1	U16	7-SEG C.A.	7-Segment Common Annode Display	
21	1	U17	IDT72241	4Kx9 bit FIFO 20ns	
22	1	JP1	POWER SUPPLY	Three Pin Power Connector (+5V & Ground)	
23	28	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C29,C30,C31,C32,C33,C34, C36,C37	.1UF	.1UF Decoupling Capacitor	
24	3	C22,C23,C24	470UF	470UF Electolytic	DigiKey P6230
25	1	C21	2200UF	2200UF Electolytic	DigiKey P6232
26	1	R1	390	390 Ohm 1/4 Watt Resistor	
27	1	R2	5.6K	5.6K Ohm 1/4 Watt Resistor	
28	2	R4,R5	75	75 Ohm 1/4 Watt Resistor	
29	1	R7	100	100 Ohm 1/4 Watt Resistor	
30	1	R3	200	200 Ohm 1/4 Watt Resistor	
31	1	R6	500	500 Ohm 1/4 Watt Resistor	
32	2	C25,C28	.047	.047UF Ceramic Disc Capacitor	
33	2	C26,C27	.1	.1UF Ceramic Disc Capacitor	
34	1	C35	1UF	1UF Ceramic Disc Capacitor	
35	1	JP2	DIN 3	3 Pin Mini-DIN connector	
36	2	R8,R9	300	300 Ohm 1/4 Watt Resistor	