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WASHINGTON UNIVERSITY IN ST. LOUIS

McKelvey School of Engineering
Department of Mechanical Engineering and Materials Science

Thesis Examination Committee:
Erik Henriksen, Chair
Sang-hoon Bae
Swami Karunamoorthy

Fabrication of Two-Dimensional Material-Based Nano-Capacitors using Bismuth Selenite (Bi_2SeO_5) to Study its Dielectric Properties

by

Sushant KC

A thesis presented to the McKelvey School of Engineering
of Washington University in partial fulfillment
of the requirements for the degree of
Master of Science

May 2024
St. Louis, Missouri

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Sushant (Major) KC

Washington University in St. Louis

May 2024

Dedicated to Ms. Ganga Pradhan

Ms. Pradhan was my 7th-grade science teacher. To me, she is not just a teacher who taught well, but a teacher who inspires children around her to become the best of themselves and more. She is the earliest inspiration for me to pursue my career in science. Thank you so much, ma'am. Words could never do the justice of describing my sincere gratitude towards you.

ABSTRACT OF THE THESIS

Fabrication of Two-Dimensional Material-Based Nano-Capacitors Using Bismuth Selenite (Bi_2SeO_5) to Study its Dielectric Properties

by

Sushant KC

Master of Science in Materials Science and Engineering

Washington University in St. Louis, 2024

Professor Eric Henriksen, Chair

In recent years, the demand for high-performance micro and nanodevices has surged, necessitating the exploration of novel dielectric materials to replace conventional silicon dioxide. Following the continuation of the Moorse law, as device dimensions reduce to nanoscale levels, the properties of silicon dioxide can degrade, leading to issues such as increased leakage current and reduced gate control. Materials with superior electrical properties, such as higher dielectric constant, lower leakage current, and better thermal stability allowing for the development of faster, more efficient, and more reliable devices are in higher demand than ever. Two-dimensional layered semiconductor nanomaterials represented by compounds such as bismuth selenite (Bi_2SeO_5) have promising potential due to their unique electrical and mechanical properties. In contrast to the conventional micro and nanoelectronic devices that use silicon-based dielectrics, bismuth selenite's high-*k* dielectric property can allow the fabrication of devices that can store more electric charge and can help with reduced power consumption, increased speed, and overall improvement of the device performance. The high dielectric value for Bi2SeO5 can open the possibility of overcoming the challenges faced during the scaling of sub-ten nanometer technology

for ultrathin silicon channels. Motivated by a recent academic paper where bismuth selenite is suggested as an alternative dielectric material with a high dielectric constant '*k'* value of 16, this paper investigates the reproducibility of these claims. In this paper, we explore the fabrication process for two nanocapacitors using bismuth selenite as a part of the dielectric stack and compare the extracted dielectric values to the findings from the recent academic literature. We find that the dielectric constant across two fabricated devices were 3.5 and 4.1 respectively, and did not align with the claims from the academic literature. The device fabrication is an attempt to explore nanofabricated capacitors with the potential of lowering the gate voltage, more efficient gate-field penetration, and power consumption in 2D electronics and integrated circuits.

Chapter 1: Introduction

The semiconductor industry is a crucial sector responsible for the designing, manufacturing, and distribution of semiconductor devices, which are the building blocks of modern electronics and technology. Some of these semiconductor devices include capacitors, transistors, diodes, integrated circuits (ICs), and microprocessors, among others. The global market for semiconductors is projected to reach $1 trillion by 2030, up from $600 billion in 2021, based on estimates made by McKinney & Company. [1] In recent years, the push for innovation within the realms of the semiconductor industry has incentivized the industry to investigate areas such as the 2-dimensional fabrication methods and 3-dimensional vertical stacking process to design better devices for the future. However, as device size continues to decrease, various issues follow these efforts for innovation. In this paper, we will be fabricating two nano-capacitor devices using a two-dimensional-based material known as Bismuth Selenite (Bi_2SeO_5). The devices will then be tested and studied to determine their dielectric constant values.

1.1 Background and Motivation

The dielectric constant is a fundamental property of a material and plays a pivotal role in the device performance of capacitors therefore, the dielectric materials used in nano-capacitors can significantly influence their performance. Based on conclusions from the research paper by X Dong, et al. (2024), titled "Exploring the high dielectric performance of Bi_2SeO_5: from bulk to bilayer and monolayer", the team reported a dielectric constant of 16 for Bismuth Selenite (Bi_2SeO_5), highlighting its relevance for nano-capacitor fabrication. This thesis aims to capitalize on the insights from previous studies on Bismuth Selenite's dielectric properties to fabricate nano-

capacitor devices. By delving into material synthesis, device fabrication, and performance characterization, in this paper, we seek to investigate the reproducibility of these claims. We explore the fabrication process for two nanocapacitors using bismuth selenite as a part of the dielectric stack and compare the extracted dielectric values to the findings from the academic literature above. The device fabrication process is an attempt to explore nanofabricated capacitors with the potential of lowering the gate voltage, less interfacial scattering, more efficient gate-field penetration, and power consumption in 2D electronics and integrated circuits.

1.2 Prior Relevant Work

Before deciding to make direct measurements with the capacitance for this thesis, our team at Dr. Henriksen's lab investigated the Hall measurements of the graphene device with a Bismuth Selenite flake in between the graphene and the gate. Based on the results, for graphene on 300 nm of SiO2, the slope value was smaller, and if we modeled the SiO2 and Bi2SeO5 as being two capacitors in series, with BSO thickness of 100 nm, then it needs a relative dielectric of 4 to work in this situation. Prior to that, we also noticed high density values, equivalent of applying ~290 volts to a regular graphene sample, which wouldn't occur unless it involved a dead sample. Overall, the change in density by applying a gate voltage is the same as for a regular graphene-on-oxide device. But the implied charge doping is very high. [2] Therefore, after these results, we have decided to perform a direct measurement through capacitance.

1.3 Overview

1.3.1 Bismuth Selenite (Bi_2SeO_5)

Bismuth Selenite belongs to the family of oxyselenides, which are compounds containing both oxygen and selenium. Bi_2SeO_5 typically crystallizes in a monoclinic crystal structure. At the molecular level, Bi_2SeO_5 consists of bismuth atoms bonded to selenium and oxygen atoms. The arrangement of these atoms in the crystal lattice determines the compound's properties, including its optical, electrical, and structural characteristics. Bi_2SeO_5 has garnered considerable attention as a van der Waals (vdW) layered dielectric material featuring excellent electrical insulation properties. From recent research, based on the first-principles calculations, the dielectric performance of Bi_2SeO_5 has been determined, showing a high average dielectric constant (ε) of >20 ranging from bulk to bilayer and monolayer. Moreover, the claims of high ε of monolayer Bi_2SeO_5 surviving under tensile or compressive strains up to 6% have been made, which greatly facilitates its integration with various 2D semiconductors and Bi_2SeO_5 ultrathin films can serve as excellent atomically flat encapsulation and dielectric layers for high-performance 2D electronic devices. [3]

Fig 1: Sample image of Bi2SeO5 used for the device fabrication for this thesis.

The Bi2SeO5 sample shown in the image above was obtained from Peking University, China, and was the sample used for this research, on which the devices were fabricated.

1.3.2 Dielectric Materials and Dielectric Constants

Dielectric materials exhibit poor conductivity due to the absence of loosely bound or free electrons capable of conducting electricity by drifting through the material. The presence of electrons is essential for facilitating the flow of electric current in a dielectric material. Electric current typically moves from the positive to the negative terminal, or vice versa, through the movement of free electrons from the negative to the positive terminal. Dielectric materials, however, support dielectric polarization, a phenomenon crucial for their function as dielectrics rather than conductors. When subjected to an electric field, dielectric polarization occurs, causing positive charges to shift in the direction of the electric field while negative charges move in the opposite direction. This polarization generates a robust internal field, effectively diminishing the overall electric field within the material. [4]

The dielectric constant of a material, represented by 'k', is a measure of how well the material can store electrical energy in an electric field compared to a vacuum or air. It represents the extent to which the material can polarize in response to an applied electric field. A material with a higher dielectric constant can store more electrical energy per unit volume compared to a material with a lower dielectric constant under the same conditions. [5] Materials with high dielectric constants are often used in capacitors to increase their capacitance without increasing their physical size. In this paper, to obtain the dielectric constant value of Bismuth Selenite, a thin film capacitor is constructed. The dielectric constant is then determined by comparing the capacitance of this capacitor with the test material.

1.3.3 Leakage Current

Leakage current in semiconductors refers to the unintended flow of electric current that occurs through a semiconductor material or device under certain conditions. Primarily there are two types of leakage current. Reverse Bias Leakage Current occurs when a reverse bias voltage is applied across a semiconductor junction, like a diode or transistor. Despite the expectation of current blockage, a small flow persists due to factors like minority carrier diffusion and generation-recombination processes. Subthreshold Leakage Current is prevalent in MOS (Metal-Oxide-Semiconductor) and this type of leakage arises when the transistor operates below its threshold voltage. Even though the transistor is intended to be off, a slight current can persist due to carrier diffusion and tunneling through the gate oxide. A high dielectric constant material can store more charge per unit area for a given voltage, resulting in a lower electric field across the dielectric layer. A lower electric field reduces the probability of carrier tunneling through the dielectric, thus decreasing leakage current. [6]

1.3.4 Gate Control/ Gate field penetration

Gate-field penetration in semiconductors refers to the ability of an electric field applied to the gate electrode of a transistor or a capacitor to effectively control the flow of charge carriers within the semiconductor channel. The higher dielectric constant of the insulating layer translates to a higher capacitance per unit area. This higher capacitance allows for greater charge accumulation in the semiconductor channel for a given gate voltage, facilitating more effective control over the channel conductivity and carrier concentration. [7]

1.4 Moore's Law

Moore's Law is a principle in the field of semiconductor technology, formulated by Gordon Moore, co-founder of Intel Corporation, in 1965. It originally stated that the number of transistors on a semiconductor chip doubles approximately every two years, leading to a doubling of the chip's performance and capabilities while reducing its cost per transistor. [8]

Moore's Law represents the rapid technological progress, and miniaturization in semiconductors, driving exponential computing power growth. It influences industry practices, leading to innovations in materials, device design, and manufacturing and remains a catalyst for innovation in the semiconductor industry.

Chapter 2: Fabrication Process for 2D-Material-based Nano-capacitors.

This chapter goes through the fabrication process involved in the preparation of the devices used during this research. The process involves a series of steps starting with mechanical exfoliation, substrate preparation, optical inspection, atomic forces microscopy, optical lithography, physical vapor deposition, chemical liftoff, and wire-bonding & soldering. Each of the processes involved is explained in detail below.

2.1 Substrate Preparation via. Mechanical Exfoliation

Mechanical exfoliation is a process used to extract thin layers of materials by mechanically cleaving or peeling off thin sheets or flakes from a bulk material crystal. This technique is often used in the production of two-dimensional materials due to its simple and cost-effective reasons. The process typically involves using adhesive tape or a similar method to repeatedly peel layers from a bulk crystal. As the layers are peeled off, they become thinner until reaching the desired thickness, typically consisting of only a few atomic layers or nanometers in thickness.

Crystal flakes of Bi2SeO5 were mechanically exfoliated using scotch tape and were deposited onto 1cm x1cm diced boron-doped silicon wafers. Different variations in peeling techniques were implemented to find the effective technique to yield the highest quality of flakes on the substrate. Flakes peeled at a medium speed with an angle of around 45 degrees from the substrate yielded the best results.

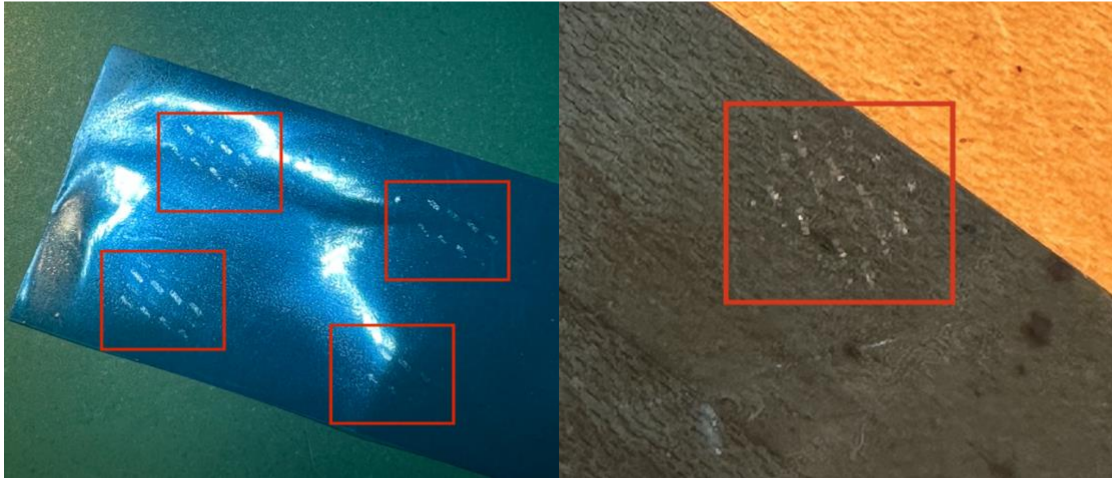

Fig 2: Crystal flakes of Bismuth Selenite exfoliated on a scotch tape surface before the depositing it into the silicon substrate.

2.2 Optical Microscope Inspection

After completing the deposition of Bi2SeO5 on the silicon substrate, the substrate was reviewed under an optical microscope to find large Bi2SeO5 flakes with uniform thickness. This is very important since the measurement of the dielectric is based on the capacitance equation and the yield results are inversely affected by the overall thickness of the Bi2SeO5 flakes.

$$C = \mathrm{k}\,\varepsilon\mathrm{o}\frac{\mathrm{A}}{\mathrm{d}}$$

Where,

‘k’ is the dielectric constant,

‘ε_o’ is the permittivity of free space,

‘A’ is the surface area of the Bi2SeO5 flake

‘d’ is the flake thickness,

Since the thickness plays a significant role in determining the capacitance of a material. Therefore, uneven, damaged, and multi-layer Bi2SeO5 were avoided by optical inspection.

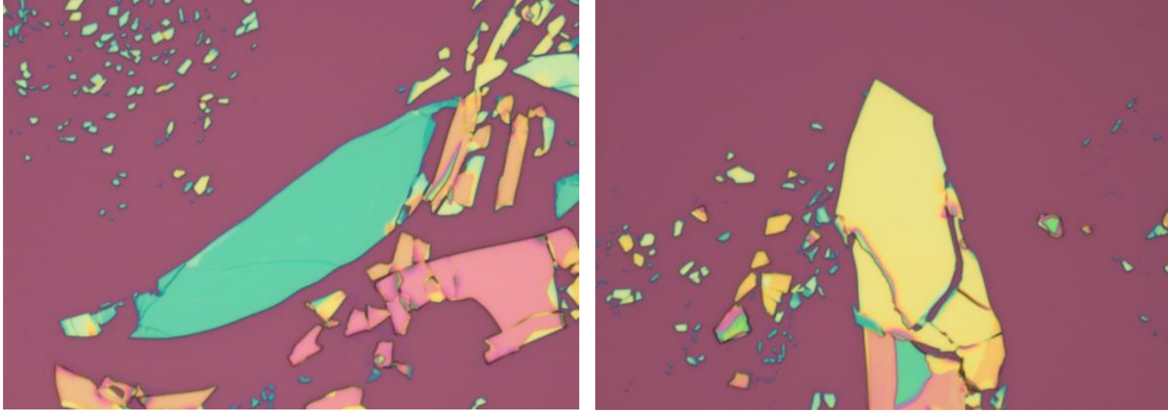

Fig 3: Images of sample flakes under 50x magnification selected for the device fabrication. Device 1 (left), Device 2 (right).

2.3 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a high-resolution imaging technique used in nanotechnology, materials science, and biology to obtain detailed surface information at the atomic level. It works by scanning a sharp tip (probe) across the surface of a sample while measuring the interactions between the tip and the surface. The Bi2SeO5 flakes from the selected sample substrates were then measured using an AFM to determine the flake thickness. Only the samples with flake sizes under 85 nanometers were considered for the device fabrication process.

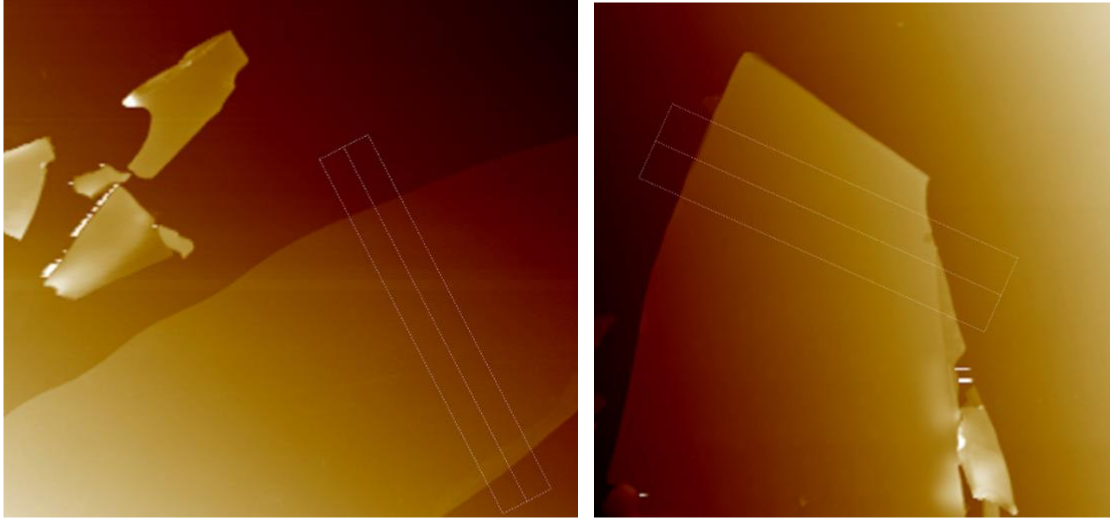

Fig 4: Atomic Force Microscopy (AFM) scans of Bi2SeO5 samples from Figure 3, that were considered for the device fabrication process. [Device 1 (left) & Device 2 (right)]

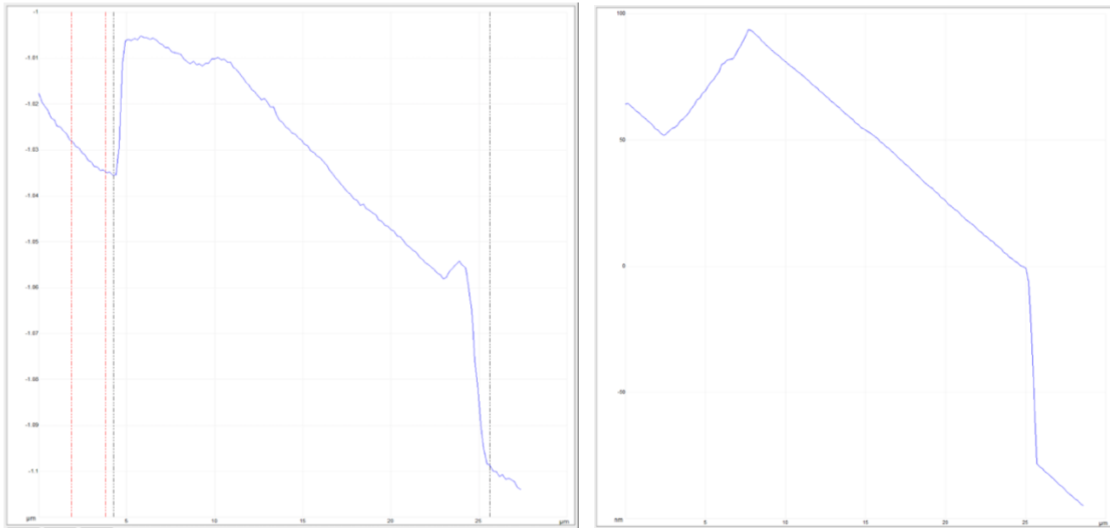

Fig 5: Corresponding Atomic Force Microscopy (AFM) thickness measurements of Bi2SeO5 samples presented in Figure 4, that were considered for device fabrication for the thesis. [Device 1, left (35nm) & Device 2, right (80nm)]

Based on the obtained results from the AFM analysis of the samples above, the table below represents an approximation of its thickness.

Measured Sample	Thickness (appx.)
Device 1	35 nm
Device 2	80 nm

Table 1: List of measured thickness for Bismuth Selenite flake for device fabrication.

2.4 Lithography

Lithography is a key process in semiconductor manufacturing that is used to transfer desired patterns onto a substrate, typically a silicon wafer for the fabrication of integrated circuits (ICs) and other micro and nano-devices. It involves using light to define intricate patterns on a photo-sensitive material called a photoresist. These patterns guide subsequent steps in the semiconductor manufacturing process, such as etching, doping, and deposition. Primarily there are two types of lithography processes; Optical lithography and Shadow Lithography. Optical lithography projects light or energy sources directly into the substrate and mostly uses positive photoresists for imprinting the pattern. Meanwhile, shadow lithography uses a mask to project light or energy in the desired location to produce the desired pattern onto the substrate. For the fabrication process in this thesis, we are using an optical lithography process with a combination of two positive-tone photoresists.

2.4.1 Spin Coating & Photoresist

The substrate must be spin-coated using appropriate photoresists before drawing the pattern using the laser writer. For the device fabrication of this paper, the sample substrates were

spin-coated using three layers of two different photoresists. LOR-1A and S1805 were the photoresists used in the process and are both positive tone photoresists. Positive tone photoresist is a type of photosensitive material used in photolithography processes that becomes more soluble in developer solution when exposed to light or energy source.

Initially, the LOR-1A photoresist was spin-coated at 4000 rpm for 60 seconds to obtain around 100nm thickness. The substrate sample was then baked at 190ºC for 5 minutes and was spin-coated again using LOR-1A photoresist under the same parameters of 4000 rpm for 60 seconds to obtain an additional 100nm of resist thickness and was baked for another 5 minutes at 190ºC. Finally, the substrate sample was then spin-coated using S1805 photoresist at 4000 rpm for 60 seconds to obtain an additional 500nm photoresist layer thickness and was baked at 125ºC for 1 minute. The RMP and thickness reference for the spin-coating were taken from each company's respective photoresist solution datasheet and are presented below. The total photoresist thickness at the end of the spin coating process on the substrate was about 700nm thick.

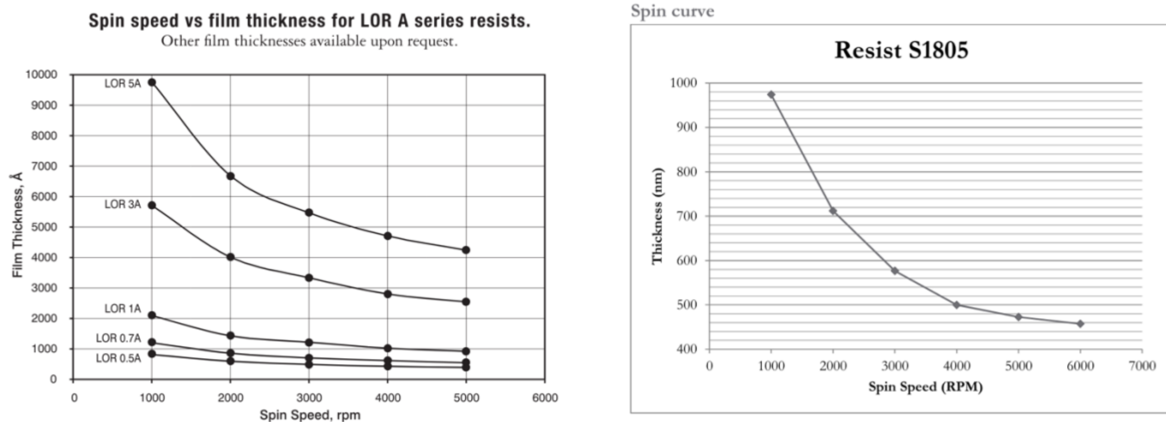

Fig 6: Respective spin-curve data sheets for photoresist LOR 1A (left) [9] and S1805 (right).[10]

2.4.2 Computer-Aided Design and Laser Writer

After spin coating the sample substrates using the required photoresist with the desired thickness, the desired pattern was drawn on the substrate sample using the Heidelberg Laser Writer. The pattern measurements were taken using the optical microscope system, and the print design for the sample substrate was designed in SOLIDWORKS. The file was then exported under the .dxf extension and uploaded to the laser writer for the lithography process.

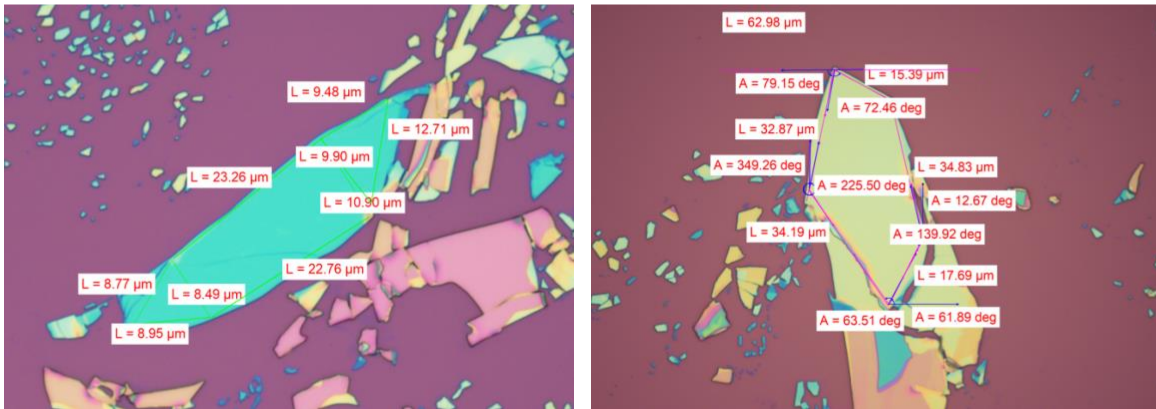

Figure 7: Measurements of the sample flakes (device 1, left) (device 2, right) for designing of the laser writer file for optical lithography.

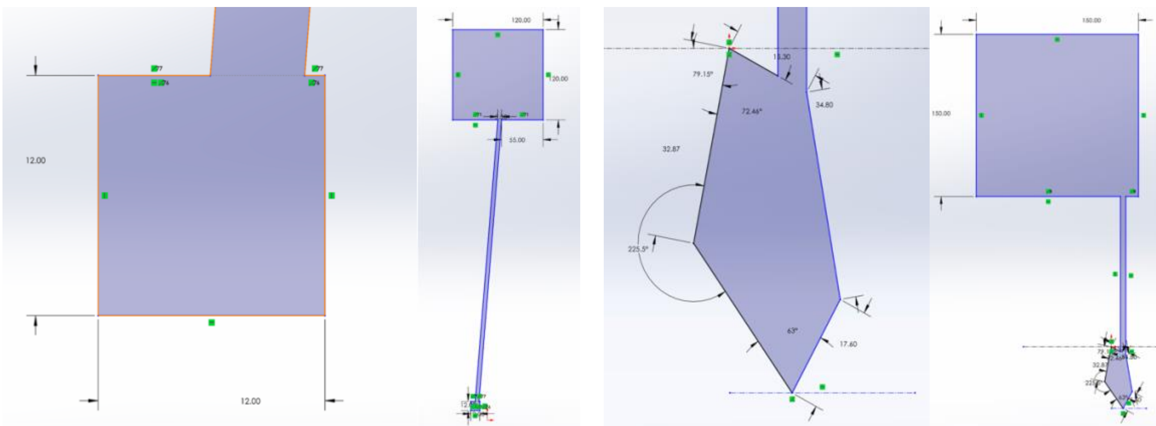

Figure 8: SOLIDWORKS designing of the laser-writer file based on the measurements taken from Figure 6.

The laser writer was then used to imprint the design shown above in *Figure 8* onto the sample substrate. A does test was initially performed on a different LOR-1A and S1805 resist spin-

coated substrate to determine the ideal parameters to obtain maximum accuracy while using the laser writer. Upon inspection, the ideal parameters to yield the highest resolution under 2mm laser-head were determined. The parameters are presented in the table below:

Power (mW)	Intensity (%)	Filter (%)	Focus (%)
42	60	5	-80

Table 2: Parameters set for the Laser Writer process to obtain highest resolution.

2.4.3 Development

Post laser writer procedure, the sample substrates were collected and developed in MIF-319 developer solution for 60 seconds, followed by another 60 seconds of deionized (DI) water and dried using compressed nitrogen air. The sample substrates were then collected and observed under an optical microscope to confirm the proper development of the pattern in the substrate. Upon inspection of the substrate that was not fully developed, additional development for 15 seconds in the developer solution was added, followed by 30 seconds in deionized water. This process was repeated until the pattern was fully developed under the optical microscope.

2.5 Physical Vapor Deposition using Thermal Evaporator

Post-development, the sample substrates underwent the Physical Vapor Deposition (PVD) process via a Thermal Evaporator. PVD is a thin film deposition technique used in micro and nanofabrication processes that involves the deposition of thin films of materials (usually metals) onto substrates through physical processes, such as evaporation or sputtering, rather than chemical reactions. A thermal evaporator is a type of PVD system and operates based on the principle of

thermal evaporation where metals are heated to very high temperatures. These metals then evaporate and deposit around the wall layers, where we can attach our sample substrate to obtain thin layers of material deposition. The deposition thickness is determined by the evaporator based on input power, timing, and metal density that needs to be deposited.

Figure 9: The interior walls of the PVD-Thermal Evaporator.

Through this process, a 5nm layer of chromium was initially deposited on the substrate. This was then followed by a 70nm thick gold layer deposition. Chromium was initially deposited between gold and the sample substrate to establish a better bond between the substrate and gold. The parameters for this process were based on the material density and the desired thickness of the metal and were performed by the IMSE cleanroom facility manager.

2.6 Liftoff

The thermal evaporator process was then followed by the liftoff process where the sample substrate was treated with PG-Remover solution for about 90 minutes at 65ºC temperature to liftoff undesired photoresist and the gold deposition layer from around the sample substrate. The substrate was then cleaned using an IPA solution, followed by deionized water, and dried using compressed nitrogen air.

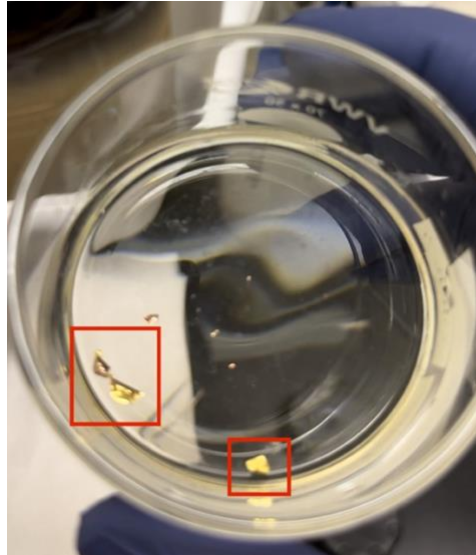

Figure 10: Metal (gold & chromium) residue in the PG-remover solution post lift-off process.

2.7 Wire-bonding & Soldering

Following the lift-off process, the substrate was then attached to the Mk 6 universal sample Printed Circuit Board (PBC) puck consisting of a total of 18 pins. The wire was bonded across the electrode pads to the pins of the PCB. The base of the sample substrate was exfoliated using a diamond-tip scribe and was soldered to a few terminals of the 18 pin puck. The exfoliated sample avoided wire bonding since it is harder for the wire to remain attached to the uneven exfoliated surface.

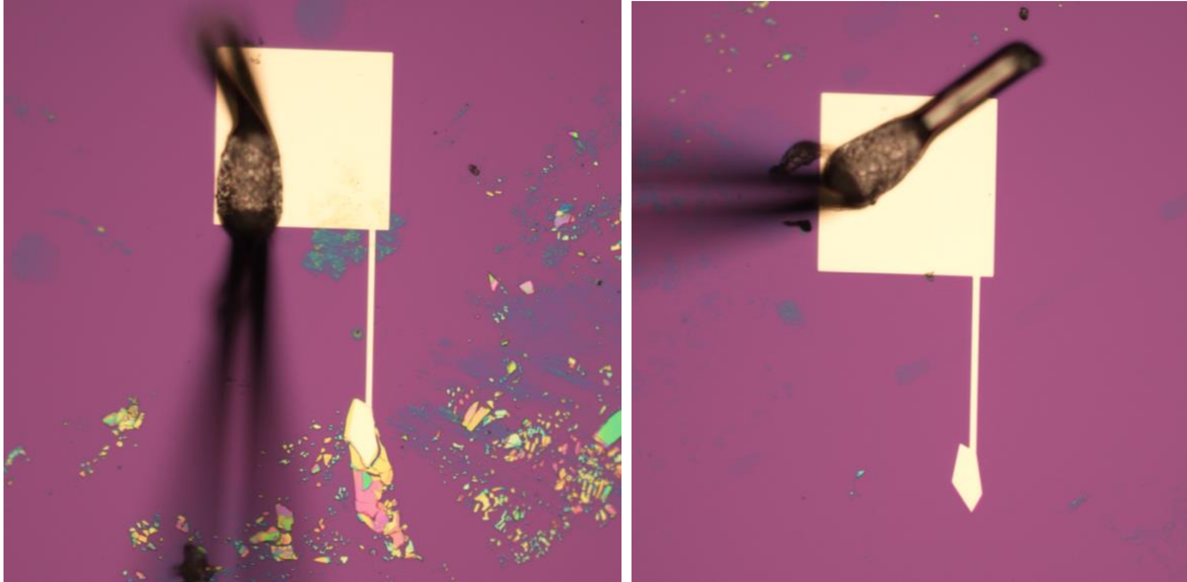

Fig 11: Wire-bonding performed to the electrode pads of Device 2 on the Bi_2SeO_5 sample (left) and SiO_2 surface (right).

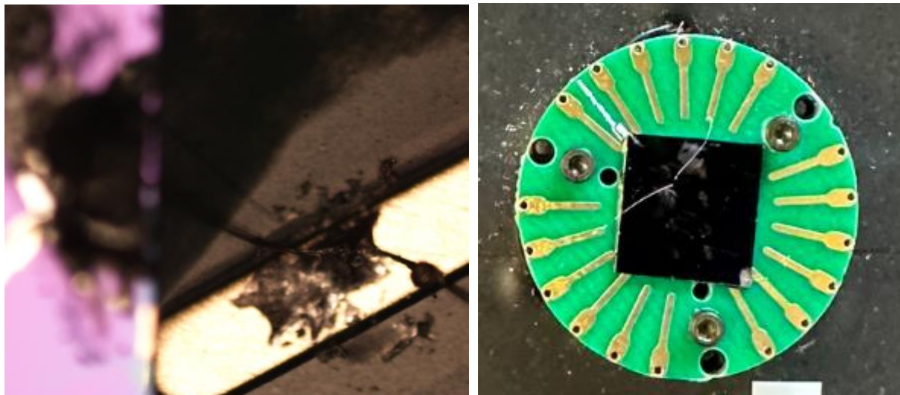

Fig 12: Microscopic image of soldering performed between the exfoliated surface of Device 1 (pink surface) and the PBC pin (left) and the complete device (right).

Chapter 3. Device Structure and Characterization

Following the completion of the device fabrication process, this chapter highlights the overall structure of our nano-capacitor device, its characterization, and the measurements.

3.1 Device Structure

Each of the two fabricated devices have two different structural composition. The first composition is the capacitor with silicon dioxide (SiO_2) as its dielectric. This is a simple composition that acts as a capacitor and can be represented by the equation below.

$$C = k\,\varepsilon o \frac{A}{d} \quad (1)$$

Where,

k is the dielectric constant,

ε_o is the permittivity of free space,

A is the surface area of the Bi2SeO5 flake

d is the flake thickness

The second structural composition is of a capacitor in series consisting of two dielectric materials i.e. silicon dioxide (SiO_2) and bismuth selenite (Bi_2SeO_5) stacked on top of one another. This composition can be represented by the equation below.

$$\frac{1}{C_{total}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{Bi_2SeO_5}} \quad (2)$$

Where,

C_{total} is the total capacitance,

C_{SiO_2} is the capacitance of silicon dioxide,

$C_{Bi_2SeO_5}$ is the capacitance of bismuth selenite.

3.2 Electrical Property Characterization

Both the devices were individually connected onto the breakout box. A multimeter was then used to find connection within the device and the breakout box ports, and finally, the setup was connected to the SR830 lock-in amplifier system. The SR830 was connected to the computer system and was used to generate specified frequency at pre-determined voltage, while measuring and recording the current across the system.

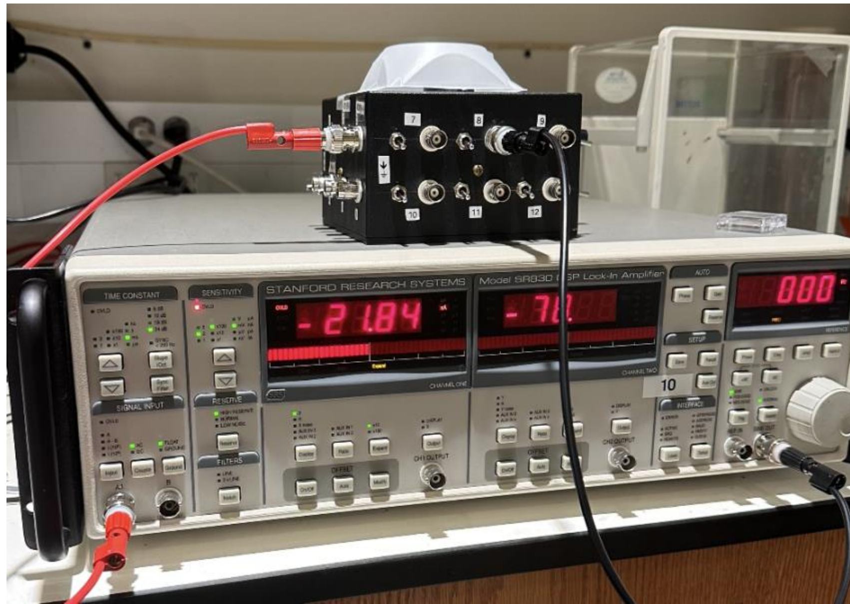

Fig 13: Connection setup of the sample device connected to a breakout box, connected to the SR830 lock-in amplifier system.

3.2.1 Current vs Frequency Measurement

Once the setup was established, a voltage of 0.01V was applied across the device at multiple frequency points. Based on the input frequency, the following parameters were set for the device measurement using the following equations;

$$Period(s) = \frac{1}{Frequency\ (Hz)} \tag{3}$$

$$Time\ Constant(s) = 3 * Period(s) \tag{4}$$

$$Data\ Interval\ (s) = 10 * Time\ Constant\ (s) \quad (5)$$

Based on these parameter settings, the following points were set to record the current vs frequency plot.

Frequency (Hz)	Period (s)	Time Constant (s)	Data Interval (s)	File Size
10 Hz	0.1s	0.3s	3s	1000
25 Hz	0.04s	0.12s	1.2s	1000
100 Hz	0.01s	0.03s	0.3s	1000
1000 Hz	0.001s	0.003s	0.03s	1000
5000 Hz	0.0002s	0.0006s	0.006s	1000
12000 Hz	0.000083	0.00025s	0.0023s	1000

Table 3: Assigned parameters for generating Current vs Frequent plot for the fabricated devices.

3.2.2 Dielectric Constant Characterization

The slope generated from the current vs frequency plot above was used to obtain the dielectric constant of Bismuth Selenite. The plots obtained from Device 1 and Device 2 are presented below, respectively.

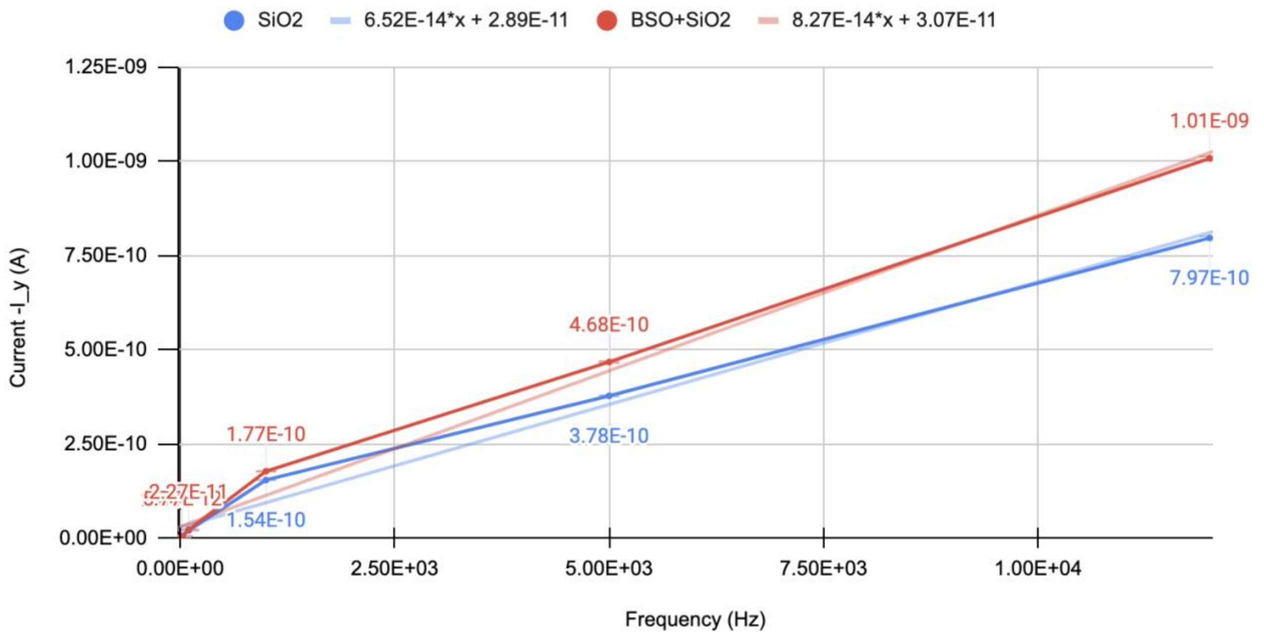

*Fig 14: Current vs Frequency measurement for **Device 1** across Bi_2SeO_5(BSO)+Si flake and SiO_2(Si) flake.*

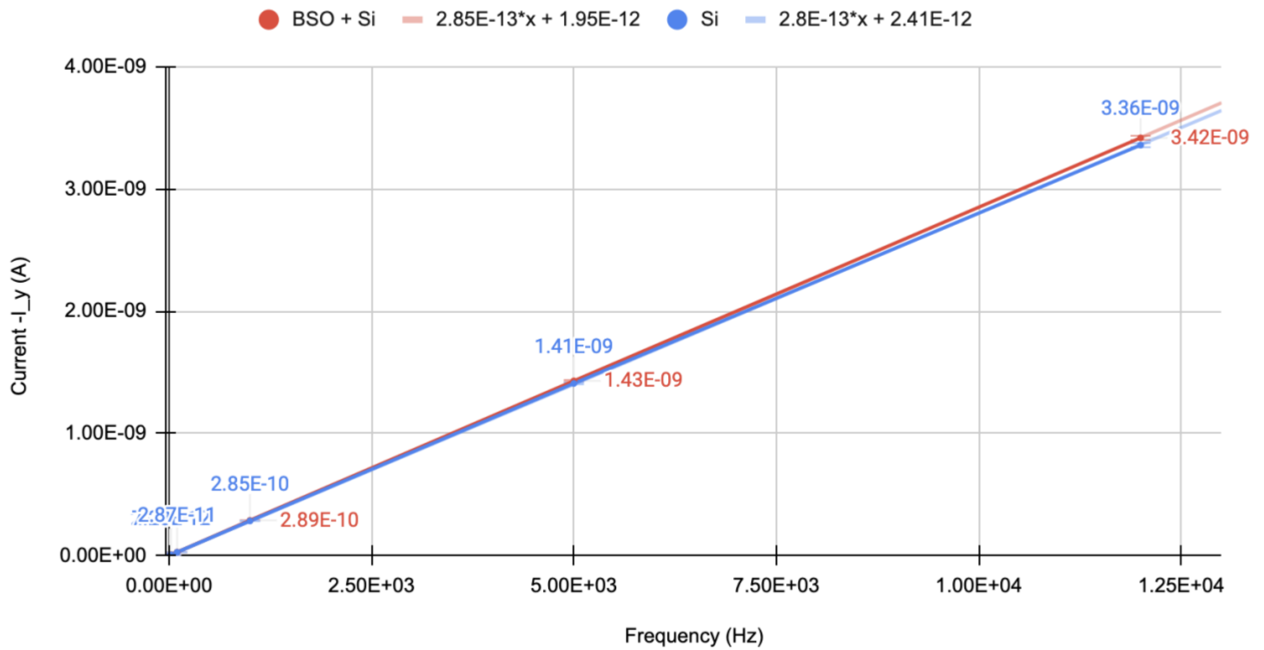

Fig 15: Current vs Frequency measurement for ***Device 2*** *across Bi_2SeO_5 (BSO)+Si flake and SiO_2 (Si) flake.*

The slope of the trendline obtained from the each of the graphs above were then calculated using eq. (1) and eq (2), alongside the derivation below, to determine the dielectric constant values for Bi_2SeO_5 and SiO_2 for both the devices respectively.

Using impedance of a capacitor in an AC circuit relation,

$$Z = \frac{1}{j\omega C} \tag{6}$$

Using the Ohm's law relation on impedance,

$$V = IZ \tag{7}$$

Combining Eq. (6) and (7), we get,

$$C = \frac{I}{f} * \frac{1}{2\pi V} \tag{8}$$

Where, Slope (m) = $\frac{I}{f}$

Combining Eq. (1), (2), and (8), and reducing capacitance of SiO_2 from the capacitance of Bi_2SeO_5 we get,

$$C_{Total,B} - C_{Total,S} = [\frac{1}{C_{flake,B}} + \frac{1}{C_{flake,S}}]^{-1} - C_{flake,S} \tag{9}$$

Finally, Eq. (9) can be solved to determine the dielectric constant values of Bi_2SeO_5 and SiO_2. Based on the calculations, the table below represents the generated dielectric constant values for Bi_2SeO_5 and SiO_2 form device 1 and device 2 respectively.

	K_{SiO2}	**$K_{Bi2SeO5}$**	**$m_{SiO2+Bi2SeO5}$**	**m_{SiO2}**
Device #1	3.7	3.5	8.27e-14	6.52e-14
Device #2	3.9	4.1	2.85e-13	2.8e-13

Table 4: Calculated dielectric constant values from Device 1 and Device 2 for Bi_2SeO_5 and SiO_2 dielectric materials.

Chapter 4: Conclusion

In conclusion, this study investigated the dielectric properties of Bismuth Selenite across two nano capacitor devices, revealing dielectric constant values of 3.5 and 4.1, respectively. The dielectric constant values for Silicon dioxide were calculated to be 3.7 and 3.9 across device 1 and device 2 respectively. These values resonate with the established values of Silicon dioxide but the dielectric constant values of bismuth Selenite do not resonate anywhere around the claimed value of 16. Despite extensive research and meticulous experimentation, the observed discrepancies persist. Several factors might contribute to these inconsistencies, including variations in sample preparation, measurement techniques, environmental conditions, and inherent material properties. A major factor that may contribute to the discrepancy of data could be the sample quality and crystalline structure. We are not sure if the sample sent to us from Peking University, China was from the same batch that was produced for their previous literature. Referring back to *Prior Relevant Work* section, this could potentially be a dead sample. Data on x-ray diffraction can be shared to confirm the crystalline structure of the materials are the same and are produced in the same conditions. The unexpected disparity between the obtained results and the literature underscores the importance of continued exploration and scrutiny in the field of dielectric materials.

Chapter 5: Future Work

Regarding the course for future work in the domain of Bismuth Selenite's (Bi2SeO5) dielectric property research, several critical routes with each offering potential for deeper exploration and understanding can be investigated. Amidst these routes, one area is the confirmation of the crystalline structure of Bismuth Selenite utilized in high dielectric constant experiments. Such confirmation lays the groundwork for unraveling the intricate interplay between crystalline structure and material properties, thereby facilitating a more comprehensive understanding of Bismuth Selenite's electrical and mechanical behavior across various structural configurations. One promising avenue for further investigation lies in the characterization technique X-ray diffraction to probe the crystalline structure and properties of Bismuth Selenite. By subjecting Bismuth Selenite samples to X-ray diffraction analysis, invaluable insights can be garnered into the spatial arrangement of atoms, lattice parameters, and crystal symmetry, thus shedding light on the underlying structural factors governing material behavior. Moreover, the identification and characterization of dead samples represent a pressing concern that must be addressed for the future research endeavors. The prevalence of dead samples poses a significant challenge to the reliability and reproducibility of experimental findings, underscoring the importance of robust quality control measures and validation protocols. By implementing stringent criteria for sample selection and verification, researchers can mitigate the risk of encountering dead samples and ensure the integrity of their experimental data. Our experimental samples were sourced directly from Peking University, China, and additional information and confirmation regarding their origin and batch consistency can provide valuable information on expectations for device performance. In conclusion, the future of Bismuth Selenite research holds immense promise, and while the results produced from our device did not necessarily align with the claims

made on the academic paper, further exploration should be initiated to understand the reason for our thesis results not aligning with the experimental data claims.

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