Report Number: WUCSE-2003-3

2003-02-01

Process Portable Analog Design

Jason R. White

Modern day digital integrated circuit designs can be designed without choosing a target programmable device or fabrication process until near the very end of the design flow. Current analog design tools and processes, however, require that the fabrication process be chosen very early on in the design process. This paper describes a vision of analog design that can be used to make more of the analog design process independent of which fabrication process is going to be used by designing at a higher, process independent level. An integrated circuit for capacitive level sensing is described and portions of the... Read complete abstract on page 2.

Process Portable Analog Design

Jason R. White

Complete Abstract:

Modern day digital integrated circuit designs can be designed without choosing a target programmable device or fabrication process until near the very end of the design flow. Current analog design tools and processes, however, require that the fabrication process be chosen very early on in the design process. This paper describes a vision of analog design that can be used to make more of the analog design process independent of which fabrication process is going to be used by designing at a higher, process independent level. An integrated circuit for capacitive level sensing is described and portions of the design are used to show how this vision allows not only for the target process to be chosen later in the design cycle, but also for comparison between processes which can help in choosing a more appropriate fabrication process.

2003-3

Process Portable Analog Design

Authors: White, Jason R.

Abstract: Modern day digital integrated circuit designs can be designed without choosing a target programmable device or fabrication process until near the very end of the design flow. Current analog design tools and processes, however, require that the fabrication process be chosen very early on in the design process. This paper describes a vision of analog design that can be used to make more of the analog design process independent of which fabrication process is going to be used by designing at a higher, process independent level. An integrated circuit for capacitive level sensing is described and portions of the design are used to show how this vision allows not only for the target process to be chosen later in the design cycle, but also for comparison between processes which can help in choosing a more appropriate fabrication process.

Type of Report: Other

Process Portable Analog Design

Jason White

Jason White, “Process Portable Analog Design,” Master’s Project, Technical Report WUCS-2003-3, Department of Computer Science and Engineering, Washington University, Saint Louis, MO, 2003.

Department of Computer Science and Engineering
Washington University
Campus Box 1045
One Brookings Dr.
St. Louis, MO 63130-4899

Process Portable Analog Design

Jason White, Washington University, St. Louis, MO
February, 2003

Abstract

Modern day digital integrated circuit designs can be designed without choosing a target programmable device or fabrication process until near the very end of the design flow. Current analog design tools and processes, however, require that the fabrication process be chosen very early on in the design process. This paper describes a vision of analog design that can be used to make more of the analog design process independent of which fabrication process is going to be used by designing at a higher, process independent level. An integrated circuit for capacitive level sensing is described and portions of the design are used to show how this vision allows not only for the target process to be chosen later in the design cycle, but also for comparison between processes which can help in choosing a more appropriate fabrication process.

1. Introduction

Although analog integrated circuit (IC) design has been around longer than digital IC design, the design flows, tools, and techniques for digital IC design have developed and progressed much more quickly than those for analog IC design. The techniques and tools currently available for digital IC design allow for a single design to be implemented in a Field Programmable Gate Array (FPGA) from different IC manufacturers or in an Application Specific Integrated Circuit (ASIC) fabricated in different processes by changing how the back-end tools are run and which design libraries are used; this can be done near the end of the design process. For example, if two numbers should be added together in a design, then the statement 'c <= a + b' will automatically result in the configuration shown in Figure 1. The designer does not have to worry about the underlying configuration. Regardless of target process, the implementation of the tools will produce the correct result for c.

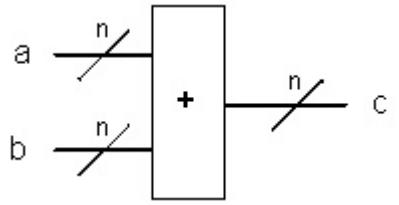

Figure 1. Block Diagram of an N-bit Adder.

In analog IC design, however, current tools and techniques require completely different designs for each fabrication process. Thus, when designing an analog IC, the target

manufacturer and process must be chosen early in the design cycle. Figure 2 graphically compares current analog and digital design flows.

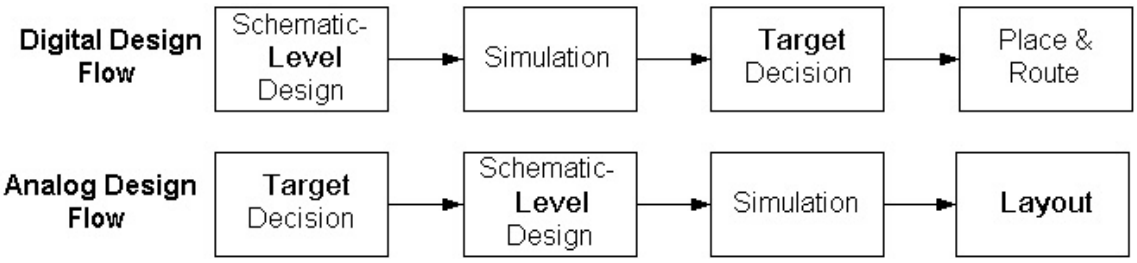

Figure 2. Comparison of Current Digital and Analog Design Flows.

In this paper, we describe a vision for analog IC design that allows for the choice of target manufacturer and process to be pushed back in the analog design cycle. This technique can also be used to compare, at a high level, the performance of an analog design in different fabrication processes without having to do completely independent designs for each process. An integrated circuit for capacitive level sensing is used to illustrate this design technique. A description of the integrated circuit will be given, while providing examples of how the design technique can be used. We also report on the current state of analog design techniques as presently supported by existing tools[1], pointing out improvements that are required for the vision to become a reality.

2. Background

An Integrated Circuit (IC) for Capacitive Level Sensing, shown at a high level in Figure 3, was designed as part of a Master's Thesis at Southern Illinois University Edwardsville (SIUE) under the direction of Professor George Engel [1]. There are four main subcomponents to the design: the voltage reference, the charge-to-voltage converter, the delta-sigma modulator, and the two phase clock generator. The voltage reference component produces two voltage references, a 3.6V reference and a 1.8V analog ground reference. The two phase clock generator produces a square wave for both phases of the clock. The charge-to-voltage component detects the charge on an external capacitor and converts it to a corresponding voltage level, which is then converted to a bit stream output by the delta-sigma modulator.

Subsequent to the thesis work, the IC was fabricated through MOSIS™ in the AMI 0.5 micron process. Testing done by Becs Technology, Inc. on the fabricated chip has revealed that the chip is sensitive to shunt resistance caused by moisture build-up on the printed circuit board (PCB). It has also been shown that the IC does not perform correctly over the entire desired temperature range (i.e., the voltage reference subcircuit does not operate at temperatures greater than 40° Celsius).

[1] The problems with analog design tools mentioned in this paper are based on the Cadence™ design tools. Some of the problems described may not exist in other analog circuit design tools.

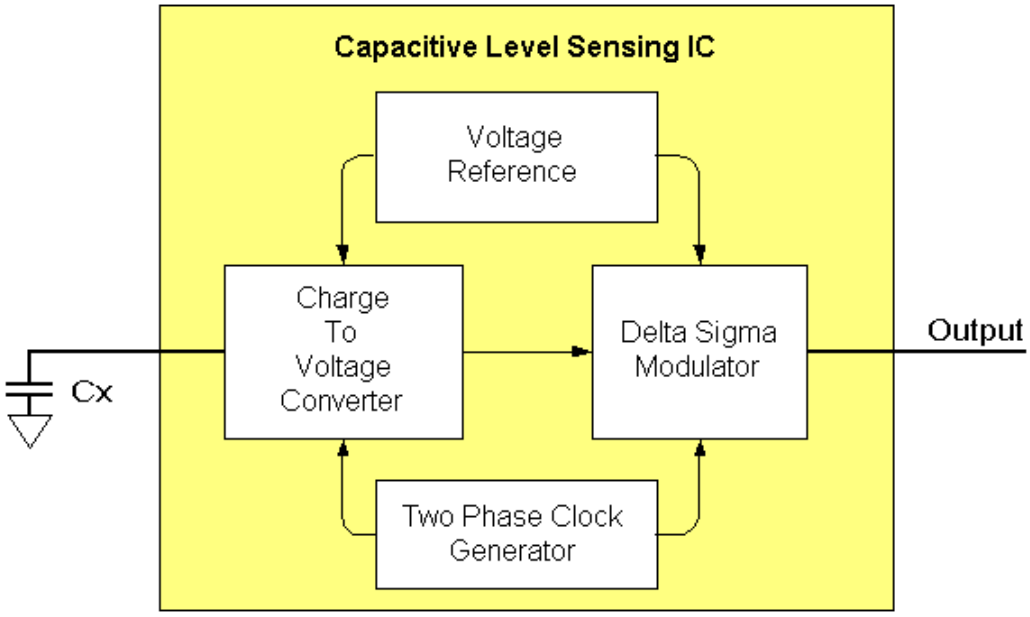

Figure 3. Block Diagram for the Integrated Circuit for Capacitive Level Sensing.

The development of the IC was motivated commercially for two reasons. First, when paired with a microcontroller, it is part of a two-chip solution to a number of capacitive level sensing and proximity detection applications that are particularly cost sensitive. A discrete component design based on similar techniques [2, 3, 4] is currently in production and is sold in a number of markets. Second, the digital circuitry and analog circuitry can be fabricated together on a single chip, forming a System-on-Chip (SoC), which results in a potentially even more cost effective system. In this case, the existing IC serves as a test chip, verifying the operation of the analog subsystem prior to integration into a larger chip that also includes the digital functions.

In this project, a model of a modified version of the IC has been created using the Cadence™ design tools. The new design includes one major change and several minor changes. The major change was in the design of the Operational Transconductance Amplifier (OTA). Instead of receiving a reference voltage, it now receives a bias current and generates the reference voltage internally. Minor changes include the addition of a multiplexor and a select line to choose between two different external unknown capacitances and the modification of how an external capacitance can be added to control the range of external capacitances that the chip can monitor.

3. Design Vision

The SoC design is prototypical of many designs, where a small analog component (e.g., sensor, actuator, A/D converter, D/A converter) is integrated onto a chip with a potentially large set of digital functionality. The capacitive level sensor described in this paper and Magneprint™ [5] are just two examples of this.

The first step towards making the analog design process portable is to use a Hardware Description Language (HDL) for modeling. Currently there are at least two HDLs that can be used to model analog circuits, Verilog-A HDL and AVHDL, both of which are language extensions to digital HDLs, Verilog and VHDL, respectively. In order to use the same HDL model for comparison of fabrication processes, careful thought should be put into the models so all the necessary pins needed for a transistor-level layout are present, even if they are unused for the HDL model, and differences between processes are parameterized, allowing for the parameters to be tuned to the appropriate values when simulating in one process versus another.

The Verilog-A model below, of a simple OTA, shown in Figure 4, shows how the transconductance (g_m) and output resistance (r_o) can be tuned depending on the fabrication process. When the OTA is simulated with g_m=100e-6 Siemens, the OTA has a gain of 80 dB, as shown in Figure 5, and when the transconductance is tuned to 50e-6 Siemens, the OTA has a gain of 74 dB, shown in Figure 6.

```
// VerilogA for BecsLib, ota_w_agnd, veriloga

`include "constants.h"
`include "discipline.h"

module ota_w_agnd(AGnd, Ib, Outp, Vdd, Vss, in_neg, in_pos);
inout AGnd, Ib, Outp, Vdd, Vss, in_neg, in_pos;
electrical AGnd, Ib, Outp, Vdd, Vss, in_neg, in_pos;

parameter real gm = 100e-6 ;
parameter real ro = 10e3 / 100e-6 ;

analog begin
  if(analysis("static")) begin
    @(initial_step) begin
      V(Outp, Vss) <+ V(AGnd, Vss) ;
    end
  end

  I(Outp) <+ V(Outp, AGnd)/ro - gm*(V(in_pos) - V(in_neg)) ;

  if(V(Outp, Vss) > V(Vdd, Vss)) V(Outp, Vss) <+ V(Vdd, Vss) ;
  if(V(Outp, Vss) < 0.0) V(Outp,Vss) <+ 0.0 ;
end
endmodule
```

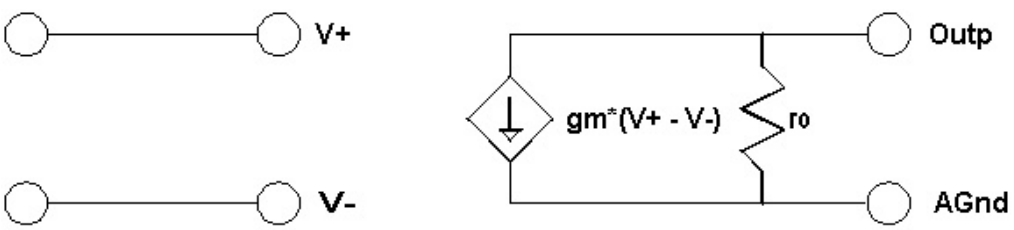

Figure 4. Model of an OTA.

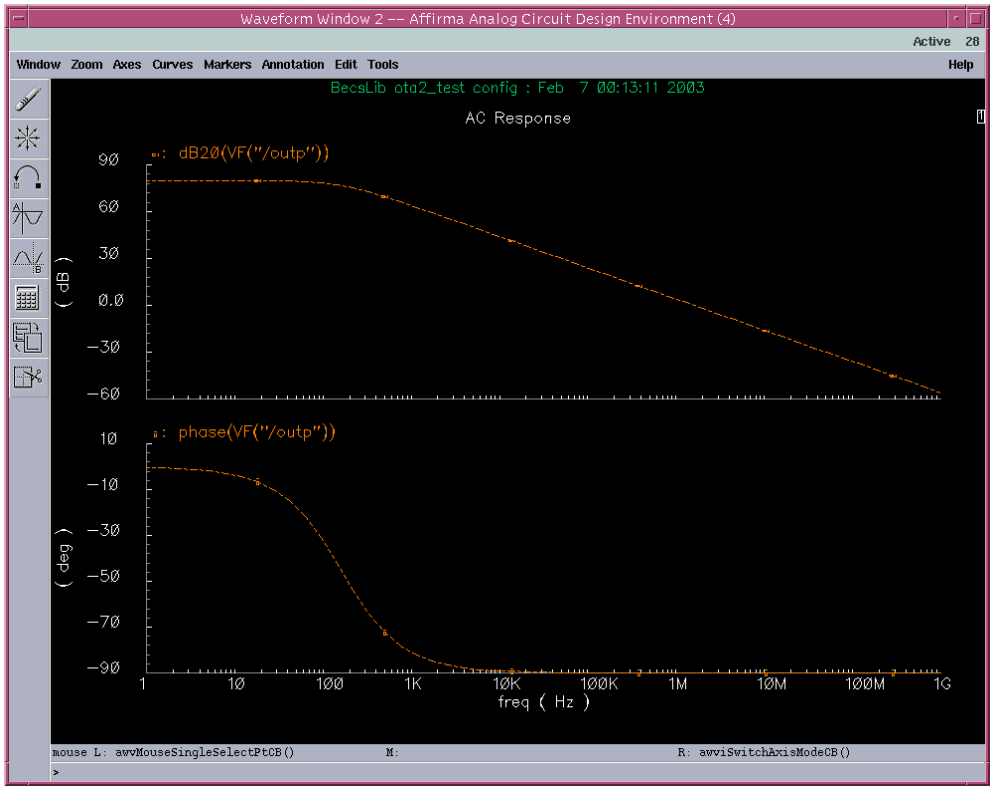

Figure 5. AC Response of the OTA with Transconductance Parameter, g_m, set to 100e-6 Siemens.

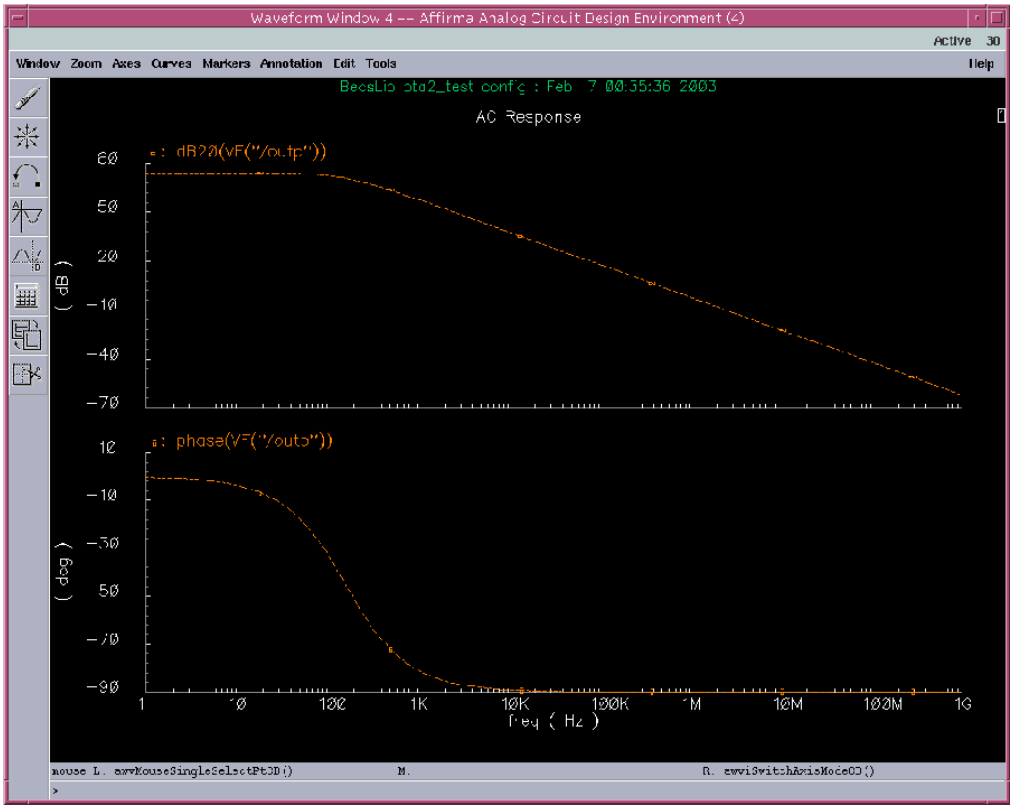

Figure 6. AC Response of the OTA with Transconductance Parameter, g_m, set to 50e-6 Siemens.

The point of this exercise is to illustrate the ability to form an abstraction barrier between the use of predesigned components (e.g., an operational transconductance amplifier) and the design and implementation of those components. An analogy can be made with the classical techniques for designing these types of systems at the board level. A system designer selects appropriate analog components (e.g., op-amp, instrumentation amp) from a library of available components (i.e., off-the-shelf ICs available from a vendor) and performs the system design without the need to know how the component is constructed internally. The designer's concern is primarily with the specifications of the component as communicated via the data sheet.

In the design space of SoCs, a system designer would like to be able to have similar capabilities. Analog components are chosen from available libraries, the external properties (e.g., open-loop transconductance of an OTA) are communicated via the library component specification, and the system design proceeds using those properties. Ideally, component libraries could have instantiations in multiple fabrication processes, making the system design at least somewhat process portable.

Clearly the ability to provide these libraries depends strongly on the degree to which the analog design pushes the capabilities of the process. However, it is not necessary that the process portability extend all the way into particularly challenging analog designs (e.g., RF components for 2.4 GHz band radios). Many SoC designs place relatively modest requirements on the analog subsystem, for example reading low-frequency sensors and performing A/D conversion.

It should also be noted that a model that is "too ideal" can cause problems with the simulator, even for simulation purposes only; ideal components can lead to the simulator being unable to resolve currents or voltages. For example, the code for a switch, shown below, caused the simulator to be unable to resolve the initial values in the charge-to-voltage circuit when the off resistance (Roff), which is process dependent, was set to 1e12 Ohms. By reducing Roff to a more realistic 1e8 Ohms, however, the simulator had no problem. From a digital view point, this is extremely unlikely. A digital simulation simply doesn't fail if one of its components is ideal, such as a non-synthesizable component; however, this can (and does) happen frequently in the current analog design tools.

```
// VerilogA for BecsLib, phs_sw, veriloga

`include "constants.h"
`include "discipline.h"

module phs_sw(Inp, Outp, Vdd, Vss, phs, phs_bar);
inout Inp, Outp, Vdd, Vss;
electrical Inp, Outp, Vdd, Vss;
input phs, phs_bar;
electrical phs, phs_bar;

  parameter real Vth=2.5 from (0:5) ;
  parameter real Ron = 1k from (0:inf) ;
  parameter real Roff = 1e8 from (0:inf) ;
  parameter real tr=10n from [0:inf) ;
  parameter real tf=10n from [0:inf) ;

  real Rch ;

  analog begin
    if (analysis("static")) begin
       Rch = Roff ;
    end
    else begin
       if (V(phs) < Vth) Rch = Roff ;
       else Rch = Ron ;
    end ;

     I(Inp, Outp) <+ V(Inp, Outp) / transition(Rch,0,tr,tf) ;
  end
endmodule
```

Verilog-A, as specified by Cadence Design Systems, Inc. [6], was used for all of the modeling done in this particular design. The top level Cadence™ schematic of the design is shown in Figure 7; it contains the four major components given in the block diagram in Figure 3, as well as some surrounding logic that provides for easier testing capabilities and allows for the IC to be used in a broader range of applications. For example, the charge-to-voltage reference voltage, analog ground (or pseudo-ground), delta-sigma reference voltage, and delta-sigma input voltage can all be set to come from an external source, rather than from inside the IC.

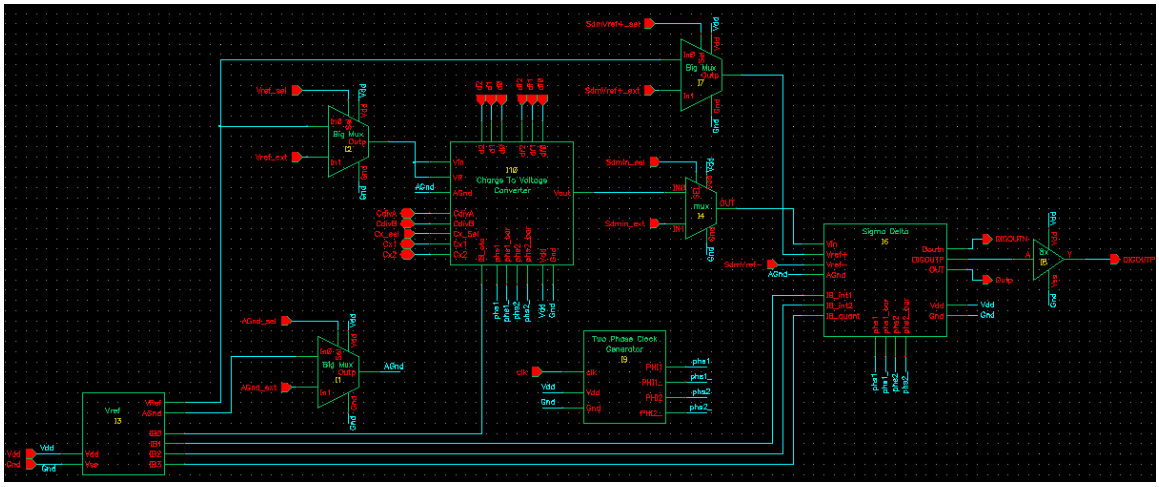

Figure 7. Cadence™ Block Diagram of the Capacitance Level Sensing Integrated Circuit.

Each block shown in Figure 7 above was modeled using Verilog-A, before transistor level schematics were prepared. The transistor-level design were prepared using libraries for the AMI™ 0.5 micron process and the XFab™ 1.0 micron process. Current tools, however, only allow a single process to be associated with a given project. A work around for this was as follows. Before launching the tools, set which technology is desired in a configuration file, and then create a new schematic in the given technology. This allowed access to the symbol, Verilog-A model, and schematic for the specified process. However, to access the schematic for a different process, the tools have to be exited and the technology configuration changed before re-launching the tools.

Figure 8 shows the accessibility of views depending on whether the tools were launched with the AMI™ or XFab™ technology. Thus, in order to compare the performance between an AMI™ and XFab™ simulation, the tools had to be launched, the simulation run, the tools closed, the technology file changed, the tools launched again, and the next simulation run. There should be no reason the technology can not be changed from inside the tools.

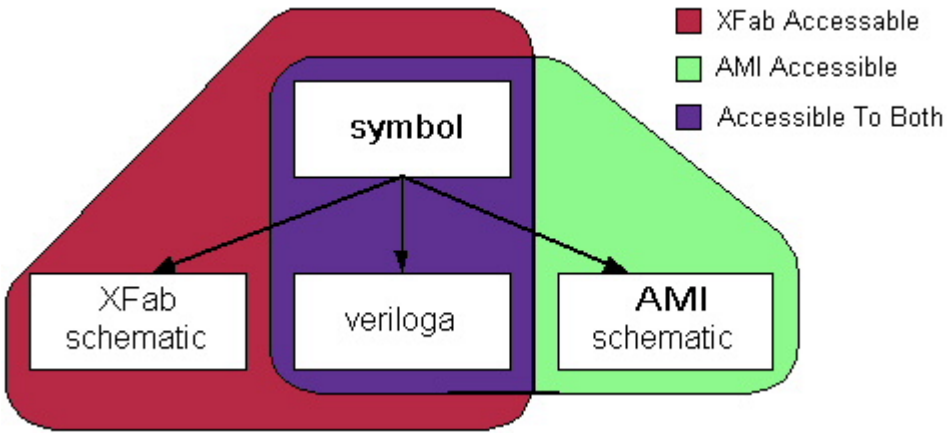

Figure 8. Diagram of Accessibility of Views Depending on which Technology Was Launched.

If the analog design tools of the future are going to allow for a single design to target multiple fabrication processes, then the tools should adapt to allow a single transistor-level design to target different processes. Instead of a fabrication company providing their own schematic libraries for the tools, the tool company should provide a standard schematic library, while the fabrication companies provide their own specifications that then get attached to the library provided by the tool vendor.

Although, it was not easy to switch between different process designs, it was rather straightforward to switch between a given process design and a Verilog-A model. Figure 9 shows the block diagram of the charge-to-voltage component. Verilog-A models were created for all five different subcomponents (multiplexor, switch, base capacitance circuit, feedback capacitance circuit, and OTA) and AMI™ and XFab™ transistor-level schematics were created for everything but the OTA. (A revised OTA design is in progress at SIUE.)

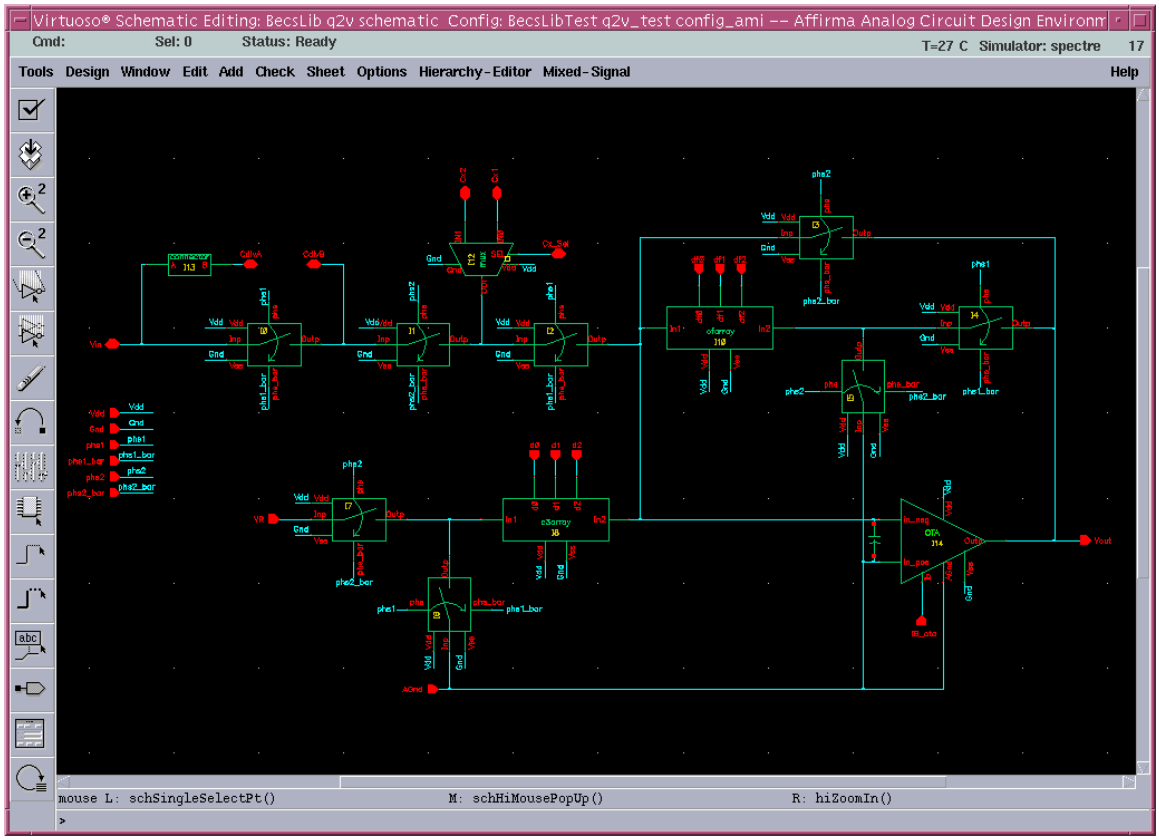

Figure 9. Cadence Schematic of the Charge-to-Voltage Component.

The charge-to-voltage component was simulated with all subcomponents using Verilog-A models, and with all subcomponents, except the OTA, using either all AMI™ or all XFab™ transistor-level designs. By using all Verilog-A models for the subcomponents, one can get an idea of how each process will perform without needing transistor-level

designs for all or any of the subcomponents by tuning the process dependent parameters in the models. Figure 10 shows the resulting data from the charge-to-voltage simulations.

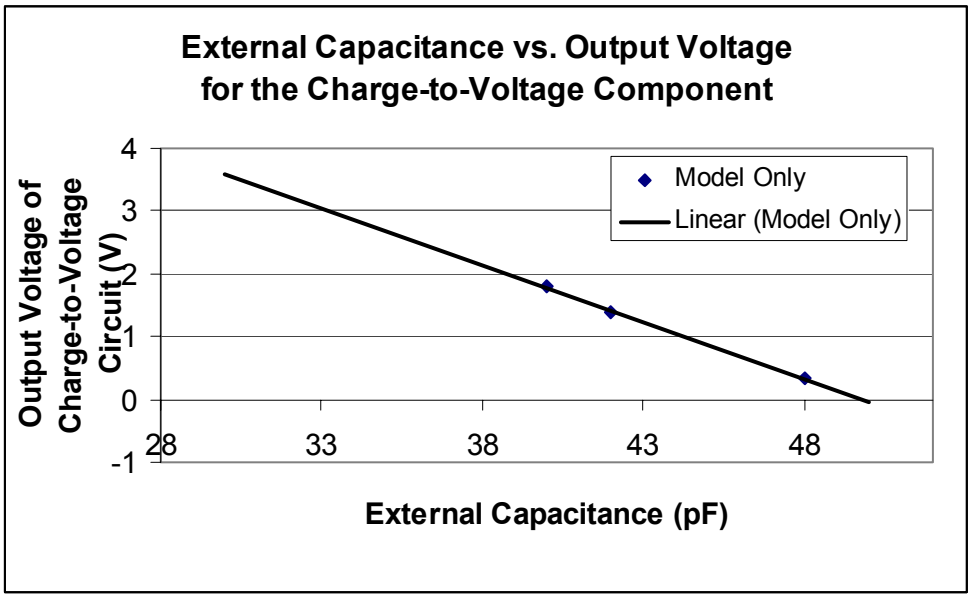

Figure 10. Results of Simulating the Charge-to-Voltage Component.

4. Future Work

Future work includes comparing performance of the entire chip in complete designs of the model, AMI™ layout, and XFab™ layout. The layout designs should also be compared to the modeled design when the parameters are all tuned to represent the given layout to see by how much they differ.

5. Conclusions

When a simple analog design is needed, the task should not be as difficult as the current tools make it. Tools for designing digital circuits continue to make the digital design cycle easier and easier; however, the tools for designing analog circuits do not appear to be improving as quickly. With a little change in how analog design tools are being developed, it should be possible for small analog designs to become less process dependent and more portable. Analog circuit design tools should be able to make small analog circuits portable between multiple fabrication processes with little extra effort on the part of the designer.

6. Acknowledgement

This work has been supported by a research grant from Becs Technology, Inc. The help and support of George Engel and Roger Chamberlain is very much appreciated.

7. References

[1] Koka, Pranay. “An Integrated Circuit for Capacitive Level Sensing”. Master’s Thesis, Southern Illinois University Edwardsville. December, 2001.

[2] David C. Macke, Sr., Richard A. Livingston, Roger D. Chamberlain, Jon G. Metcalf, “Proximity detector for hard-to-detect materials,” US Patent #6,446,012, issued September 3, 2002.

[3] Richard A. Livingston, “Balanced charge pump capacitive material sensor,” US Patent #6,362,632, issued March 26, 2002.

[4] William J. Stewart and David C. Macke, Sr., “Sensor package for proximity detectors,” US Patent #6,295,881, issued October 2, 2001.

[5] Robert S. DeLand, Jr. and Thomas C. McGeary, “Magnetic stripe card verification system,” US Patent #6,098,881, issued August 8, 2000.

[6] Cadence Design Systems, Inc. “Affirma™ Verilog-A Language Reference”. May 2001.