Fabrication And Performance Evaluation Of An Evaporative Hollow Micropillar Module For Data Center Cooling Application

Quan Harry Chau

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Fabrication and Performance Evaluation of an Evaporative Hollow Micropillar Module
for Data Center Cooling Application
by
Quan Harry Chau

A thesis presented to
the McKelvey School of Engineering
of Washington University in
partial fulfillment of the
requirements for the degree
of Master of Science

August 2022
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ABSTRACT OF THE THESIS

Fabrication and Performance Evaluation of an Evaporative Hollow Micropillar Module for Data Center Cooling Application

by

Quan Harry Chau

Master of Science in Aerospace Engineering

Washington University in St. Louis, 2022

Professor Damena Agonafer, Chair

With the exponential growth of the Internet in the coming decade, data centers will be one of the largest consumers of electricity in many countries. In many data centers, thermal management systems could be just as power-consuming as IT equipment. Chillers in these thermal management systems are one of the highest power components. Microscale evaporation is a promising approach to dissipating high heat fluxes by minimizing thermal resistance between the junction temperature and ambient temperature, hence eliminating the need for chillers. Previous research has shown that droplets elevated by micropillars can limit the vapor diffusion confinement effect, which improves the evaporative heat transfer performance.

For this thesis, an evaporative cooling module consisting of an array of hollow triangular micropillars was developed. This module allows microdroplets to be confined on top of the pillars' upper surface in optimal evaporative size. The thesis describes the device's fabrication process in a cleanroom environment, performance testing, and numerical simulations using COMSOL Multiphysics to illustrate the transport mechanisms behind our experiments.
The results show the heat dissipating capacity of different design arrangements at multiple junction temperatures. The evaporative cooling module developed in this thesis will lay the groundwork for the future implementation of this cooling technology in the next generations of data centers.
Chapter 1: Introduction and Motivation

1.1. Growing Thermal Challenges For Data Center Cooling

In the last two decades, data centers have become the backbone of our internet technology. With new robust information technologies such as AI, Machine Learning, and IoT relying heavily on cloud storage and computing, data centers will become one of the most critical facilities of human society. Companies, financial institutions, universities, and governments use data centers to store and process all the data they produce and/or collect. The demands require data centers to grow both in size and scope, making thermal management more challenging. New thermal management systems can help resolve the two biggest issues for data centers: improving computing performance and decreasing energy consumption.

1.1.1. Break through the clock speed barrier to maximize computing power

Up till the early 2000s, semiconductor manufacturers have been successfully doubling the number of transistors in a dense integrated circuit (IC) every two years to catch up with the famous Moore’s law since the 1960s. In this decade, the two years time frame is no longer feasible, but the number of transistors in IC continues to grow exponentially [1]. Along with the growth in the number of transistors, Robert H. Dennard, in a paper for the IEEE Journal of Solid-State Circuits in 1974, made an observation called “Denard Scaling” showing that when MOSFETs transistors shrink in size, their power density remains constant. In other words, with transistors getting smaller, their power consumption will also get smaller. With more transistors that can be packed into a dense integrated circuit without a significant increase in power density, the peak computing efficiency of computer chips has been doubling every 1.6 years, as observed by Koomey et al, at least until the early 2000s [2]. However, Dennard scaling came to an end
around 2006. As transistors get smaller, the ability of the manufacturer to maintain voltage to each chip at a reliable operating level becomes harder due to current leakage, which can cause static power losses that heat the chip, risking a thermal runaway that can lead to complete breakdown. Without the ability to scale down voltage, the clock frequencies of processors are limited. Most CPU manufacturers have turned to multicore CPUs to improve performance. Many workloads benefit from the greater core count, however, the increased active switching elements from having many cores still result in increased overall power consumption, worsening CPU power dissipation difficulties [3]. Therefore, in the design of modern computer systems, the power dissipation for processor chips has become one of the most crucial parameters [4]. In recent years, chip power dissipation can reach above 100 W with localized hot spot fluxes up to 1 kW/cm² [5]. With increased demands requiring high computing performance from every computer, data centers’ computers in the future will require more and more aggressive cooling strategies to break through the clock speed barrier.

1.1.2. Minimize energy consumption and global warming impact

In the US alone, data centers in the past decade have consumed around 1.86 % of all electricity produced [6]. Globally, the data center industry consumed around 286 TWh in 2016, accounting for 1.15% of global electricity [7]. With a 25% annual growth rate for Global Data Center IP Traffic, data centers are expected to consume around 3–13% of global electricity in 2030, a significant increase compared to 1% in 2010 [8]. This increase follows the general trend of the information industry which can be seen in Fig 1.
As early as 2008, the Climate Group’s SMART 2020 report estimated that the worldwide energy consumption by data centers alone in 2020 would be responsible for up to 259 metric tonnes of CO2 emissions [9]. This prediction emphasized a significant contribution to global warming as the scale of data centers continues to grow.

**Figure 1.** Energy consumption forecast of communications technology industry till 2030.
In most data centers, the chillers draw a substantial minor fraction of the electricity consumed, almost the same portion as the IT equipment itself [10]. A typical data center chiller can consume up to 33% of total electrical power as shown in Fig 2. This consumption will increase as many data centers are retrofitted with state-of-the-art GPUs, ASICS, and heterogeneous integrated semiconductor devices with increased power densities. The next generation of these semiconductor devices will soon generate heat fluxes exceeding 1 kW/cm². To ensure both high heat dissipation efficiency and low energy consumption, data centers in the future will require thermal management strategies that can dissipate heat in a more effective manner.

1.2. Traditional Cooling Methods

Forced Air Cooling is the most common cooling method for microelectronics. A typical setup involves a heatsink to dissipate the heat away from the chip and a fan set up to carry that heat away to the ambient. The flow of hot air can either be rejected directly to the environment in small, individual-scale cooling applications. However, when microelectronics are densely packed in large quantities like in data centers, rejected hot air needs to be cooled down by sub-ambient
chilled water to maintain sufficient heat transfer. The advantages of forced air cooling systems are set-up simplicity, low initial cost, and ease of maintenance [10]. In data centers, forced air cooling can also be easily incorporated into existing HVAC systems in the hot rack cool rack configuration.

However, thermal resistance between different components in forced-air cooling systems can hinder its performance, especially in high-performance applications like data centers. One high thermal resistance point is the coupling gap between the heat generating source and the heat sink. Thermal interface materials (TIM) are generally used to improve the heat transfer rate at junction points. However, these materials typically have higher thermal resistance than metallic heat sink material so a certain thickness needs to be maintained to allow sufficient adhesiveness and no air gap between two interfaces[11]. Another thermal resistance comes from the high thermal resistance between the heat sink and the ambient air within the cooling cycle. In addition to low cooling efficiency from thermal resistance, forced air cooling systems can be costly to maintain and operate due to operating at most temperatures.

1.3. Liquid Cooling and the future of thermal management

1.3.1. Single Phase Cooling

In the last few decades, liquid cooling has been extensively researched to overcome challenges with forced-air cooling and allow high heat flux to be dissipated from the next generations of power electronics. For liquid cooling, a system can either be designed to maintain a single-phase or take advantage of the phase-changing process of liquid for two-phase cooling. Although single-phase cooling can dissipate high heat fluxes (1 kW/cm) while maintaining small thermal resistances (0.1 °C/W), its efficiency is fundamentally bound by the inverse relationship between the pressure head of the coolant and the hydraulic diameter [5], [12], [13], [14].
1.3.2. Two Phase Cooling

Compared to single-phase cooling, two-phase cooling, utilizing either boiling or evaporation, is more desirable since the large latent heat of vaporization of the fluid can dissipate large amounts of heat [15]. In addition, the nearly constant temperature of the liquid-vapor mixture during the phase change process can greatly reduce the thermal resistance between the heat source and the ambient environment [16]. While flow boiling in microchannels has shown great potential for dissipating high heat fluxes [17], it presents additional challenges, including large pressure drops and flow instabilities [18], [19], [20], limiting the heat removal capacity at the critical heat flux (CHF) [21], [22], [23]. The growth and advection of vapor bubbles in microchannels increase the pressure drop due to the added friction of the two-phase flow and the acceleration of the fluid during vaporization. This increased system pressure during two-phase flow increases the required pumping power and manifests itself as an additional thermal resistance by shifting saturation conditions so that the working fluid vaporizes at a higher temperature. Static Ledinegg instabilities created by the pressure rise during two-phase flow in parallel channel systems can cause flow maldistribution, starving boiling channels of fluid and leading to earlier dry-out [24], [25],[26]. Another major challenge in flow boiling is to maintain the optimum exit quality of vapor. The vapor quality mainly depends on the inlet coolant temperature and the mass flow rate, and it can determine the different flow boiling regimes [27],[28]. The highest heat transfer coefficient is associated with the optimum vapor quality (50%–75%) [28], which has been observed during thinning of the liquid film in the annular flow regime [29]–[31]. For even higher vapor qualities, the heat transfer coefficient deteriorates until it reaches the minimum reported values, at qualities approaching unity, which are generally associated with observed dry-out conditions. When the gas volume fraction increases to more than 95% (and hence the liquid
fraction is less than 5%), the resulting liquid films attain micron, and eventually sub-micron, thicknesses that can have extremely high heat transfer coefficients. Although these ultra-thin, sub-micron liquid films offer great promise for the thermal management of high heat flux electronic components, the current literature shows that deep in the annular flow regime, as gas qualities fall well below those required to form such ultra-thin films, the heat transfer coefficient decreases sharply [32]–[34]. This decline in cooling effectiveness has been argued to be caused by the breakdown of the liquid film (film rupture) and local dry-out [32]–[34]. Additionally, high vapor quality is associated with flow fluctuations and flow by-pass, which can also contribute to lowering the local heat transfer coefficients [35]. Since the heat transfer coefficient is independent of vapor quality in the nucleate boiling regime [36], restricting boiling in the nucleate boiling regime by using micro- or nanoporous coatings can be an effective method of mitigating problems with high vapor quality. Another way is to increase the coolant subcooling so that the exit quality is limited [33], [34]. Zhou et al. proposed vapor removal through a porous hydrophobic membrane to mitigate some of the problems observed during flow boiling in microchannels [37]. The key component in the heat exchanger proposed by Zhou et al. is a porous hydrophobic membrane that, through capillary forces, prevents the liquid from leaking out of the device but provides minimal flow resistance to the vapor phase. The vapor flows through the membrane into a separate set of parallel channels on the other side. The vapor can then be reintroduced into the coolant flow downstream of the microchannels, where the impact of two-phase flow is less significant to the system. This vapor venting technology has been able to lower the pressure drop (by 60%), as well as lower the mass flux and exit quality [25]. Other methods to overcome challenges related to boiling in microchannels include the use of micronozzles and microscale cavities [38] (achieving a 55% reduction in pressure drop),
promoting the nucleate boiling regime by introducing size-controlled nucleation sites created by silicon nanowires, and avoiding reverse flow caused by the Ledinegg instability by creating a flow constriction in the microchannel [39], [40].

1.4. Bio-inspired Micropillar Structure For Evaporation Cooling

To enhance microscale evaporative heat transfer, technologies such as surface coatings, micro/nano-structures, and wicking structures to modify wettability and improve liquid spreading have demonstrated significant results. Both numerical and experimental works Kokalj et al.’s work constructed an analytical model of an array of evaporating sessile droplets on a porous membrane that mimics human sweat glands [41]. Following this research, Chakraborty et al. developed both analytical and numerical analysis on a single layer of water droplets in cooling Intel Xeon and Core i7-900 computer chips[42]. Both studies showed higher heat-dissipating performance as the density of droplets and temperatures increased. However, with the presence of a solid substrate, downward vapor diffusion of sessile droplets is hampered. This phenomenon, the so-called diffusion confinement effect, can be mitigated by suspending the droplets from the bottom substrate using a micropillar as Li et al demonstrated in their work [43]. By studying the morphology of these sessile droplets, Shan et al. and Ma et al [44], [45] achieved a 71% heat transfer coefficient on asymmetric droplets confined on hollow micropillar structures compared to spherical droplets. These asymmetric droplets have a higher perimeter-to-wetted area ratio and radius of curvature which help increase the evaporation rate. However, these past works have only focused on single droplets on single pillars.
1.5. Scope of the thesis

The research inquiries driving this thesis work were to determine the best fabrication technique to create arrays of silicon hollow micropillar structures, allowing water to flow through and water droplets to pin on top while evaporation happens at constant pressure. We also want to construct an experimental rig to obtain the heat transfer rate of this evaporative cooling module and analyze the experimental results side-by-side with the evaporation numerical models to determine the future development to improve heat transfer performance.

There are 3 types of structures reported in this presentation: circular/orthogonal arrangement, triangular/orthogonal arrangement, and triangular/staggered arrangement. All pillars have the same perimeters as a 150 um circle.

If a module can be fabricated and effectively characterized, then there is enormous potential to start industry engineers to integrate this structure into future embedded 2 phase cooling systems, opening up more options for data centers when it comes to liquid cooling.
Chapter 2: Cooling Module Fabrication

The micropillar array-based cooling modules are fabricated on a double-side polished 100 mm silicon wafer with ~900 nm thermally oxidized SiO₂, which serves as a hard etch mask for creating hollow micropillars. Silicon wafers were dry-oxidized in the tube furnace (Lindberg/Blue M) for 80 hours under 1000 degrees C. For the scope of this thesis, 300 μm thick wafers were used. Future works might require thinner wafers due to the limited etching of aspect ratio of the deep reactive ion etching mentioned later in this thesis. Figure 3 schematically shows the three-step process for fabricating a hollow micropillar array: (I) SiO₂ removal by reactive-ion etching for pre-DRIE patterning and alignment marks visualization, (II) etching through-wafer holes from the backside of the wafer, and (III) etching pillars on the front side. Figure 4 shows the 3D CAD constructed model of what the testing module would look like when fabrication is completed.
Figure 3. Fabrication process step-by-step flow chart. (I) Backside Pt RTD and heater elements. (II) Backside holes (III) Front side pillars

Figure 4. 3D CAD generated model of 2 testing modules with orthogonal and staggered pillar arrangement. A. and C. are the module cross-section at the water feeding channel of the
orthogonal and staggered arrangement, respectively. B. and D. are the transparent view to see both sides of the orthogonal and staggered arrangement, respectively.

2.1. Fabrication of RTD Sensors and heaters

We performed photolithography to pattern the deposition and etching. For this layer, a 5” inch mask(AZ1500/Cr/Sodalime glass) with a pattern like Fig.5 was used.

Figure 5. The backside of the wafer with the RTD Sensors and Heaters was fabricated.

The patterns contain the electronic components later used during the experiment: the RTD sensor and the thin film heater. To perform photolithography on this wafer, a layer of LOR 10B and a layer of S180 photoresist (PR) was spin-coated on top of the wafer. This combination of PR is reliable metal lift-off. To achieve a bubble-free layer of photoresist, LOR10B was poured into the wafer directly. S1805 is not viscous so pipet drop-casting works fine. LOR10B is not light-sensitive and is easy to be removed so it works well as the base layer lift-off. The UV exposure amount is determined by S1805 only. It is important to soft bake in between each layer
of PR since it helps to evaporate the solvent to make the PR more solid. The layer's thickness will be somewhat altered by evaporation, which will also get the PR ready for UV exposure. After finishing preparing the PR layer, we exposed the wafer to UV light at the dosage of 122.5 mJ/cm² and then developed the wafer in MF319 solution for 60 seconds. We then rinsed the wafer with a gentle flow of water to achieve a PR mask. Using this mask, we put the sample in Thermal Evaporator (Edwards 306 Vacuum Coater) to coat 20nm of Cr and 50nm of Au. The layer of Cr allows the metal composite to bind to the silicon substrate, while the Au layer provides great conductivity for the RTD sensors and the heaters.

2.2. Backside hole etching

The porous micropillars were fabricated on the same side as the pattern electronic component from the alignment marks. The process creates 25 μm diameter boreholes from the same side as the alignment marks. To begin, the wafer is cleaned using acetone, IPA, and DI water in sequence. A 16 μm layer of AZ 4620 photoresist is spin-coated at 1000 rpm onto the wafer. This layer is then exposed to ultraviolet light through the hole pattern in the mask, using a UV-LED mask aligner (KLOE UV-KUB3) at a dosage of 840 mJ/cm². The wafer is then developed in AZ 400K (diluted 3:1 in DI water) for 3 minutes. The wafer is then gently washed in DI water before being hard baked at 105 °C for 10 min and mounted in a chamber for reactive ion etching (Oxford Instruments Plasma Lab 100 System). The exposed area of the wafer first undergoes a gentle descumming with oxygen plasma to clean the surface. Then the silicon oxide layer is removed by inductively coupled plasma (ICP) etching. The recipe is C₄F₈ at 45 scc/m, O₂ at 5 scc/m, a bottom RF power of 50 W, and top power of 750 W. Mild SiO2 etch power avoids overheating the photoresist. After the process, the exposed area ends up with a layer of photoresist mask on top of the SiO2 layer. Deep silicon etching (Bosch process) then creates the
250 μm diameter straight-wall borehole. One fabrication cycle includes one deposition process (C4F8 80 sccm, RF 15 W, ICP 600 W, 8 sec) and one etch process (SF6 130 sccm, RF 25 W, ICP 600 W, 8 sec). The etching does not puncture the wafer, so the photoresist layer remains flat and smooth during front side fabrication and the photoresist does not clog the holes. The wafer is then developed in AZ 400T at 80 degrees C for 1 hour to dissolve the photoresist.

Figure 6. Optical microscope image of the sample’s backside once the DRIE is completed.

2.3. Front micropillar array fabrication

To create an array of micropillars on the front side, we first spin-coat a layer of MCC Primer 80/20 and leave it for 10 min without baking to enhance adhesion. A layer of 9 μm AZ P4620 is then spin-coated at 3000 rpm on top of the Primer layer and hard-baked for 10 minutes at 105 °C. The wafer is then loaded into a Heidelberg DWL66+ Laser writer, where the pattern of the micropillar shapes is aligned on the front to match the holes from the backside. The pattern is then laser-written on the front side at a laser power of 70 mW/cm², and the wafer is quickly
transferred into a bath of AZ 400K (3:1 ratio) to develop for 4 minutes. As with the backside, the wafer is subsequently submerged in a water bath to wash away the developer, then dried and hard-baked for 5 minutes. Next, the wafer is transferred to the RIE machine for oxide layer removal, followed by deep reactive ion etching (DRIE) to create pillars 100 μm high on the outer edge. At the same time, DRIE also creates holes in the center of the pillars that connect with the holes previously created from the backside.

**Figure 7.** Optical microscope image of the sample’s front side once the pillars are formed and completed
2.4. Fabrication challenges

2.4.1. Backside metal hard to lift off/ Peel off wrong side

Figure 8. The backside of the sample with deposition failures, from left to right: fail to lift off, deformed/shrink feature, and damaged feature.

The first major fabrication challenge comes from the metal electronics components in the back of the wafer. As you can see from Fig. 8, the metal was not well deposited, and the metal was not precisely deposited on the developed pattern. There are 3 underlying causes we suspected:

1. The metal in the back is made out of 2 components, Cr and Au. Cr plays a role in the adhesion of Au to the substrate, so after thermal evaporation deposition, the uneven distribution of Cr could have caused these bad spots. We can fix this by increasing the thickness of the Cr layer and increasing the spinning speed of the thermal evaporator to achieve more even Cr distribution. 2. At positions on the backside where metal is supposed to be lift-off, the PR underneath could still be there and was not dissolved by the stripper. We can fix this by heating the stripper to 80C for 30mins to increase the dissolving effect on PR. 3. There could be residue on the developed sites, hindering the adhesion of the metal to the substrate. The solution to fix this was to clean the wafer thoroughly before fabrication, as well as after development, making sure there is no residue.
2.4.2. Backside hole over expanded

![Image of backside holes](image)

**Figure 9.** Backside holes (outer black ring) over expanded, bigger than front side holes.

Another challenge that we soon realized once we complete a batch is that the backside hole is larger than the front side hole. The cause of this might have come from the deformation of the PR holes, causing them to be enlarged during the DRIE process.

To fix this, we hard bake the PR after development so that it will harden and maintain the diameter during ICP-RIE etching, as well as the DRIE etching.

2.4.3. Pillar being over etched
Another fabrication challenge we realized as we finish fabrication is the over-etching/tapering shape of the pillars. We suspect that this is caused by over-powerful DRIE, therefore we lowered the ICP power to 600 W instead of 750W and increase the number of cycles from 300 to 400.

We also suspected that the PR mask might be shrunk by heat during the DRIE process causing tapering. To fix this, we grow the SiO2 mask to be thicker, from 450nm to 900nm, and it would be used as the only mask for the DRIE process. The hardness and heat resistance of SiO2 should provide us with better etch selectivity.
2.4.5. High surface roughness, droplets hard to pin, and blockage inside the pores

![Before and after RCA and O₂ plasma cleaning treatment of a circular/ orthogonal arrangement sample.](image)

**Figure 11.** Before and after RCA and O₂ plasma cleaning treatment of a circular/ orthogonal arrangement sample.

One last problem we realize as we collect the sample for the experiment is that there are blockages inside pillar holes, preventing water from coming out from the pillar. We did not know why until we observe the sample under SEM and we can see a lot of debris and residue on our sample.

These come from the PR that we used that is not being fully cleaned during the fabrication process, as well as external contamination during handling and transportation. Therefore, after that batch, we conduct RCA cleaning in the end and O₂ plasma cleaning after every milestone big steps to ensure minimum residue, and prevent external heat to burn the residue, making it harder to be removed later on.

2.5. Fabrication results

Wafers after completing the fabrication process are broken down into 24 individual samples. To observe these samples, we use Environmental Scanning Electron Microscope (Thermofisher
Quattro S) available at WashU Materials Characterization Facility. A scanning electron microscope (SEM) creates images of material by scanning it with a focussed beam of electrons. The sample's surface topography and chemical composition are revealed by the signals that are created as a result of the electrons' interactions with the sample's atoms. Images of the micropillar surface were captured at various magnifications and angles. An SEM has an objective lens and a condenser lens. Instead of photographing the specimen, each lens concentrates the beam to a specific area. Depending on the required particle viewing window, the voltage was set to 1.0 kV with magnitudes of either 5.00 K or 1.00 K.

![SEM images](image)

**Figure 12.** Top View SEM image of (a) staggered arrangement sample (b) 1 pillar from the staggered arrangement sample (c) orthogonal arrangement sample.
Figure 13. (A) Isometric view of 150 μm Orthogonal Array. (B) Isometric view of 150 μm Staggered Array. (C) Isometric view of 150 μm Orthogonal Pillar. (D) Isometric view of 150 μm Staggered Pillar. (E) Side View wall of Pillars. (F) Thin-film gold RTD sensor and Heater for providing heat flux and measuring temperature during experiments.
Chapter 3: Computer Modeling & Simulations

Numerical simulations were conducted using COMSOL Multiphysics to predict the heat transfer performance of the evaporative hollow micropillar array. Due to the periodicity of the array configuration, a parallelogram unit-cell simulation model was built using Surface Evolver, Solidworks, and COMSOL. The simulations were running under steady-state conditions, with a droplet of a fixed shape and a constant evaporation rate. In the solid domain, thermal conduction is the only attribution of the heat transfer process. In the liquid domain, since the Peclet number, Rayleigh number, and Marangoni number were found to be small in this study, convection was negligible. Therefore, thermal conduction also becomes the only attribution of the heat transfer process. The conductive heat transfer in both domains is governed by the heat conduction equation, given by

$$\nabla^2 T = 0 \quad (3.1)$$

where $T$ is the continuous temperature function. A constant temperature boundary condition was assigned to the bottom of the silicon substrate. In the gas domain, the water vapor concentration was solved by the steady-state species transport equation:

$$- \mathbf{V} \cdot \nabla C_v + \nabla \cdot \left( D_{\text{diff}} \nabla C_v \right) = 0, \quad (3.2)$$

where $\mathbf{V}$ is the velocity in the gas domain driven by Stefan flow and thermal buoyancy flow. A constant concentration boundary condition was assigned at the top surface of the gas domain, and a vapor concentration boundary condition was assigned at the liquid-vapor interface. A no-penetration boundary condition was assigned to the solid-vapor interfaces. Two pairs of periodic conditions were assigned at facing surfaces of the air domain to ensure the periodicity of the unit-cell simulation.

The local evaporative flux along the liquid-vapor interface was calculated using
\[ J = \bar{M} \cdot \left( - D_{\text{diff}} \frac{\partial c_v}{\partial n} + n \cdot \nu C_v \right) \quad (3.3) \]

and the total evaporation rate was calculated by surface integral by

\[ \dot{m} = \int_S J ds, c \quad (3.4) \]

where \( J \) is the evaporative flux, \( \bar{M} \) is the molecular weight, \( D \) is the diffusion coefficient, and \( n \) is the normal vector of the interface. A heat flux boundary condition was applied at the liquid-vapor interface to satisfy energy conservation

\[ k_l \left( \frac{\partial T}{\partial n} \right)_{lv} = D h_{fg} \left( \frac{\partial c_v}{\partial n} \right)_{lv}, \quad (3.5) \]

where \( k_l \) is the thermal conductivity of water, \( h_{fg} \) is the latent heat of vaporization, \( D \) is the air-vapor molecular diffusion coefficient, and \( c_v \) is the vapor concentration at the liquid-vapor interface. The vapor concentration at the liquid-vapor interface was considered to be equal to the saturation concentration:

\[ c_{v,lv} = c_{\text{sat}}(T_{lv}), \quad (3.6) \]

where \( c_{\text{sat}} \) is the saturated vapor concentration. The velocity and temperature in the gas domain are solved by the following governing equations regards of continuity, momentum, and energy conservation:

\[ \nabla \cdot (\rho \nu) = 0 \quad (3.7) \]

\[ \rho(\nu \cdot \nabla) \nu = \nabla \left[ - \rho I + \mu \left( \nabla \nu + (\nabla \nu)^T \right) - \frac{2}{3} \mu (\nabla \cdot \nu) I \right] + \rho g, \quad (3.8) \]

\[ \rho c_v \nu \cdot \nabla T - \nabla \cdot (k \nabla T) = \rho c_v \frac{\partial T}{\partial t} \quad (3.9) \]

The temperature at the liquid-vapor interface was first solved in the liquid domain and the result was used for solving the temperature in the gas domain. The velocity boundary condition at the
liquid-vapor interface in the gas domain is given by:

\[ \vec{v}_n = \frac{1}{c_{air}} \cdot D \frac{\partial c_{air}}{\partial n} = -\frac{1}{c_p - c_v} \cdot D \frac{\partial c_v}{\partial n}. \]  

(3.10)

In this numerical simulation, the thermal buoyancy flow is considered by setting the air density as a function of the local temperature solved by the heat transfer model. The height of the gas domain is set as 50 times the height of the micropillar. At the far-field, the boundary conditions are set to 32% relative humidity at 295K.
Chapter 4: Measurement & Surface Characterization

Before the evaporation experiment began, the RTD element on the device was calibrated. The calibration method is shown in Fig. 14.

![RTD calibration process](image)

**Figure 14.** Sample’s RTD sensor calibration process (I) RTD sensor is connected to Thermometer using Kapton tape. (II) Sample in a water bath for calibration in oven

![RTD sensor temperature calibration curve](image)

**Figure 15.** RTD sensor temperature calibration curve example
A type K thermocouple was taped to the device to monitor the temperature. Wires were taped to the RTD element pads and connected to a multimeter to measure the resistance. The whole sample was then submerged in a bath of lab-graded DI water. The bath containing the sample was then transferred to an oven where we heated the whole apparatus. The temperature in the oven was raise from 30 to 140 degrees C at 10-degree intervals, each interval lasts for 30 minutes, allowing the temperature to stabilize. The temperature reading from the thermocouple and the resistance of the RTD element was recorded at the end of the 30 minutes. The relationship between temperature and resistance was then plotted to be used as the reference for the experiment as shown in Fig 15.

After calibration, the device was dried using a nitrogen gun. The device went through O2 plasma treatment for 5 minutes at 25W to remove organic contamination before wire and tubing attaching. Copper wires were attached to the RTD sensor and thin-film heater pads using silver paste (MG Chemicals, 473-1220-ND, USA). NanoPort (IDEX Health and Science, N-333, USA) connectors were aligned with the micropillar holes and bonded to the backside of the devices using J-B weld epoxy (J-B Weld, cold weld 8280, USA). The silicone O-ring inside of the NanoPort sealed the area around the micropillar holes to prevent liquid leakage during the experiment.
Figure 16. (a) Schematic drawing of the experimental setup. (b)-(e) Photograph of the experimental setup.
The experiment is set up as shown in Fig 16. The evaporation experiment system consisted of a Thorlabs manual stage system, a DC power supply (Keithley Instruments, 2231A-30-3, USA), a multimeter (Keithley Instruments, DMM7510), and 2 DSLR cameras (Canon EOS 6D Mark 2, Rebel T3) equipped with microscopic lenses to observe top view and side view. To maintain a constant pressure for droplet evaporation, a pressure regulator (Elveflow, OB1 MK3, France), which connected to a compressed nitrogen tank (outlet pressure = 280 kPa), enabled gas to flow with a stable pressure into a confined water reservoir, pushing DI water into the tubing. The flow rate and downstream flow pressure were monitored by a microfluidic flow sensor (Elveflow, MFS, range = 0–7 μL/min, resolution = 0.01 μL/min, France) and a pressure sensor (Elveflow, MPS, range: 0–6894.76 Pa, resolution: 1 Pa, France). Although DI water was boiled for 15 minutes before each experiment, to further eliminate the possibility of air bubbles, which can interfere with the flow rate measurement, a debubbler and IDEX degassing system were integrated into the system. The experiment started by pumping the DI water into the back of the sample and waiting for droplets to stabilize at certain pressure as shown in Fig 17. At the steady state, the volumetric flow rate measured by the flow sensor provides the instantaneous evaporation rate of the droplets on the device. The RTD sensor on the device was connected to the multimeter and the thin-film heater was connected to the DC supply. A data acquisition system (National Instrument, USB-6363, USA) transmitted resistance data from the multimeter to the computer to be converted to temperature using the calibration results on our Labview program.
Figure 17. Water droplets pinning on top of one row of pillars in a triangular/orthogonal arrangement.
Chapter 5: Experimental Results Discussion

The evaporation experiments are conducted under the ambient temperature of 22 ± 1 °C and relative humidity of 32 ± 5%. Since we can only directly measure the evaporation rate of the cooling module, the dissipated heat flux by evaporation can only be calculated by dividing the evaporation power by the active area which can be shown in Fig 18. Figure 19 and Table 1 demonstrate the relationship between the heat flux dissipated by the cooling module under substrate temperatures ranging from 30 °C to 90 °C.

Figure 18. The active area used for heat flux calculation is enclosed in the red boundary.

To demonstrate the full potential of the device, there are two types of heat flux conducted in this case: active area heat flux and per pillar heat flux. For the heat flux per pillar, the area used to
find the heat flux is the solid-liquid area of each pillar. The active area heat flux on \( t \) is calculated based on the flow rate measurement from the flow meter as

\[
\phi_q = \dot{V} \rho_{water} h_{fg} / A_{active} \quad (5.1)
\]

**Figure 19.** Experimental measured and numerical analysis predicted dissipated heat flux for the triangular micropillar array with a staggered arrangement using the active area formula and individual pillar area. The temperature range is 30 to 90 for the simulation and 40-85 for the experiment.
Table 1. Heat transfer coefficient and heat flux from experimental and simulation data for 150 μm staggered arrangement pillars

<table>
<thead>
<tr>
<th>Temperature</th>
<th>h [W/m2-K]</th>
<th>Q [W/cm2]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulation</td>
<td>Experimental</td>
</tr>
<tr>
<td>40</td>
<td>2.09E+01</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>2.41E+01</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>3.02E+01</td>
<td></td>
</tr>
<tr>
<td>65</td>
<td></td>
<td>1.34E+03</td>
</tr>
<tr>
<td>70</td>
<td>3.76E+01</td>
<td>3.68E+03</td>
</tr>
<tr>
<td>75</td>
<td></td>
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<td></td>
<td>4.54E+03</td>
</tr>
<tr>
<td>90</td>
<td>2.03E+03</td>
<td></td>
</tr>
<tr>
<td>98</td>
<td>3.26E+03</td>
<td></td>
</tr>
</tbody>
</table>

where the flow rate $\dot{V}$ is measured by the flowmeter, $h_{fg}$ and $\rho_{water}$ vary as water temperature changes based on the temperature of the experiment, and A is the selected area. At water temperatures between 40 and 60, the variation in evaporation rate is relatively low, leading to a relatively small dissipated heat flow density. However, starting at 60 degrees C, the dissipated heat flux begins to rapidly increase non-linearly. This phenomenon happened due to the nonlinear relationship between the equilibrium pressure and the solid-liquid vapor interfacial temperature, which can be described by the following equation:

$$c_{sat}(T_{lv}) = \frac{n_{sat}(T_{lv})}{V} = \frac{p_{sat}(T_{lv}) \cdot V / R \cdot T_{lv}}{V} = \frac{p_{satref}}{R \cdot T_{lv}} \exp \left[ \frac{M h_{fg}}{R} \left( \frac{1}{T_{satref}} - \frac{1}{T_{lv}} \right) \right]$$  (5.2)
In this equation, as $T_{lv}$ grows, so does the saturated vapor concentration, allowing for a greater concentration gradient in the vapor domain near the liquid-vapor interface. Furthermore, the vapor concentration in the far-field (ambient) is stable, and the vapor diffusion coefficient is not temperature dependent. As a result, the evaporation rate from the droplet surface increases with increasing vapor concentration ($J_{evap} = D_{diff} C_v$).
Chapter 6: Conclusion and Future Works

In this thesis, we successfully presented a complete fabrication of the hollow micropillar structure that has the ability to dispense water and sustain the asymmetric droplets on top. We also created a testing apparatus and successfully collected preliminary evaporation performance data of these micropillar structures. These preliminary results created a foundation to optimize micropillar array patterns by maximizing micropillar packing density to achieve higher dissipating heat flux.

![Figure 20. From left to right: a. Schematic of the liquid cooling mechanism, b. A 3D model concept for integrating the cooling device into a real PCB.](image)

We’re looking forward to embedding directly into high-power processors for an optimized thermal management solution in the future. Figure 20a shows how our device can work with dielectric liquid by combining direct liquid cooling and evaporative cooling for maximum heat dissipation capacity. This device’s main component is the center block which has the evaporative cooling surface. Dielectric will come in through the liquid inlet, go through the fluid delivery layer, take away the heat, and either evaporate or recirculate back for cooling in case there is a mismatch between the pumping rate and the evaporation rate. Figure 20b shows the 3D PCB
model of how the device can be integrated directly at the chipset level to minimize the thermal resistance caused by traditional chip packaging. Despite our current design, we also working with a different industry expert to transfer this idea to more manufacturable designs. The potential of this idea is proven and ready to be explored in future work.
References


