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BTC Modifications

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BTC MODIFICATIONS

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Abstract

This paper describes the modifications made to the design of the Broadcast Translation Circuit based on test results from the first fabrication run. The document updates document WUCS-89-52, which outlines the design of the BTC in full detail. This version of the BTC will be fabricated using a 2.0 μm N-well CMOS process.

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BTC Modifications

1. Introduction

This paper describes the modifications made to the design of the Broadcast Translation Circuit (BTC) based on test results from the first fabrication run. Document WUCS-89-52 describes the design of the BTC in detail. A sample fabrication run received in October 1988 had a yield of 65% at 21MHz whereas the target speed for the circuit was 25MHz. The circuit tests and simulation runs used to isolate the bottleneck are described in the next section. The results showed that it was not possible to write to the BTT at 25MHz due to a combination of slow test access points and an unacceptable delay in the signal that latched data into the BTT. All the other data paths appeared to function normally at the specified operational speed. There were other modifications made to the circuit besides fixing the bus carrying data to the BTT, all of which were in the interest of making the design more robust.

2. Device Testing & Simulation Analysis

There were two failures observed during device testing.

- Tap connections to pins on the chip failed to work at speeds above 15MHz.
- Data could not be retrieved from the BTT at 25MHz.

The problem with the taps was not critical since it did not interfere with the data path, but only with the ability to monitor it. The issue with the BTT merited close examination and a number of tests were carried out to determine what part of the BTT functionality failed.

2.1. Failure Analysis for the BTT

The Tektronix LV500 may be programmed to run different parts of an input pattern at different frequencies. A test where all write BTT packets were processed at 21MHz and all other packets processed at 25MHz, yielded correct output data. This implied that it was not possible to write to the BTT at 25MHz and also that this appeared to be the only critical malfunction in the circuit. Also, since it was possible to read data from the BTT at 25MHz, both the *pt* and address signal to it functioned correctly. This left only the upstream data path to the BTT. A block diagram of this data path is given in Figure 1.

The parity generator regenerates the signal about halfway down the path. The shift registers before the latches qualified by *mil* also perform a complete regeneration. CAZM showed that a combination of two factors may have caused the failure, and both are listed below. All CAZM results are from simulation at 42MHz because no failures were observed at lower frequencies.

- The *mil* signal was asserted during $\phi 2$, i.e. while data was changing.
- The first byte of the 4-byte serial data was not latched by *pgen* due to the set-up delay from *INC* and a slow test access point design.

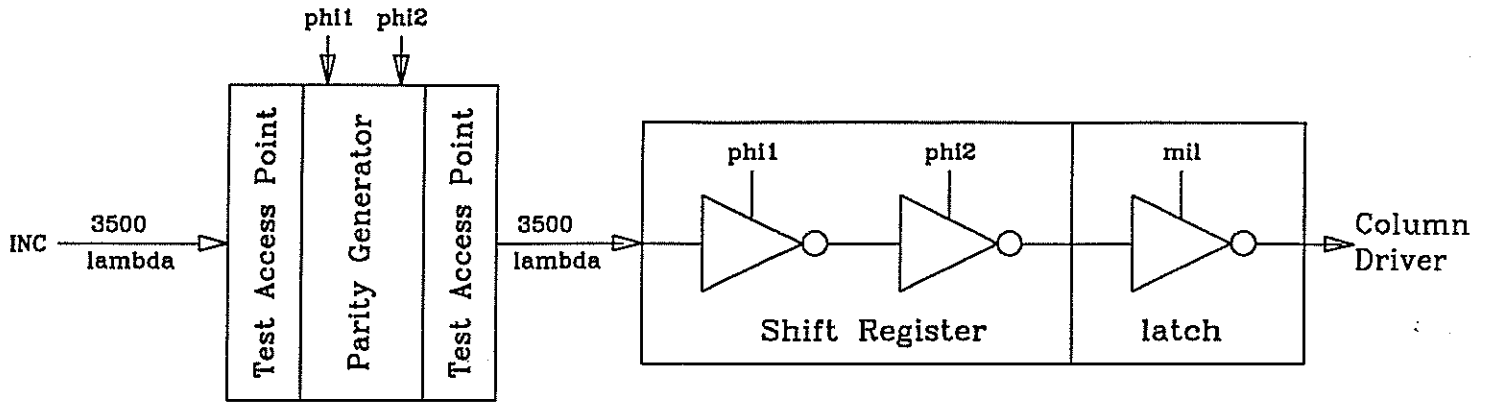


Figure 1. INC to BTT Upstream Data interface

Figure 2 shows the *mil* signal with respect to the clocks. Figure 3 shows the loss of the first byte of data. Notice that the first byte of data at the input to the parity generator arrives at the trailing edge of ϕ_1 , and pgen does not register it. Both of these factors confirmed the failure observed on the device itself.

There were two further tests performed to confirm that the two explanations for the failure observed in simulation were consistent with the device failure.

- A slower clock speed with ϕ_1 and ϕ_2 the same lengths as before and skewed so that the ϕ_{21} interval is the same as at 25MHz.
- A set-up with all 4 bytes of data to the BTT identical.

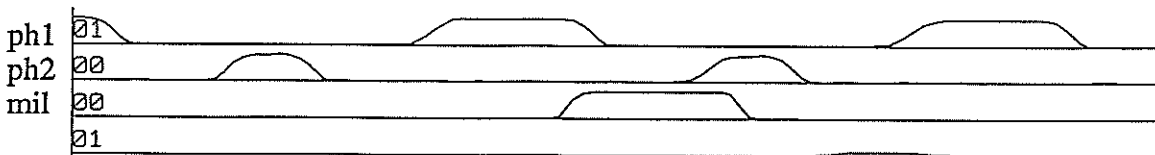


Figure 2. MIL with respect to Clocks

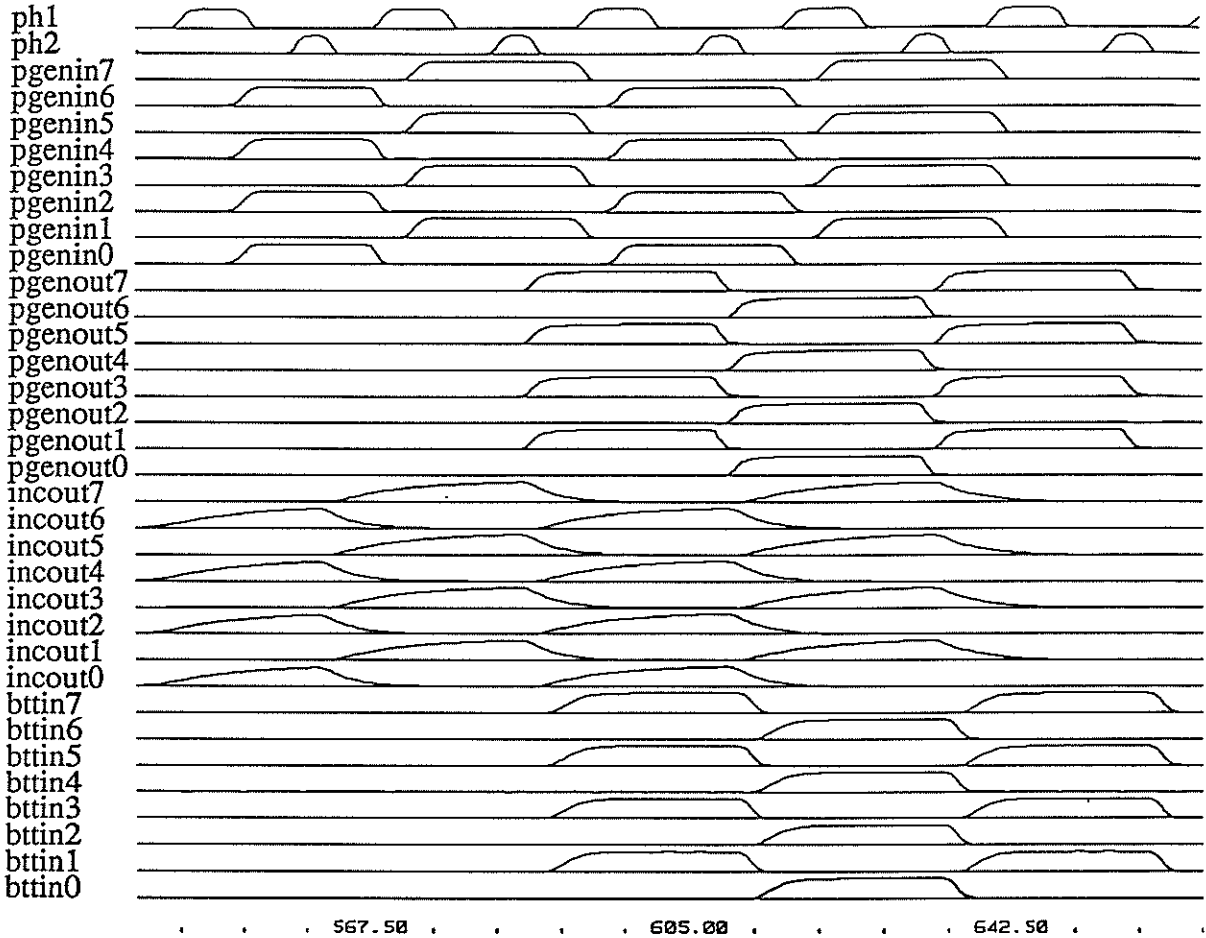


Figure 3. Loss of first byte of Upstream BTT data

The identical data test is important. When all four bytes were the same, data was read out of the BTT correctly. This works because data was not being changed while the signals were latched by *pgen* and while *mil* was asserted. It rules out the concern about the integrity of the memory cells and their control. The interval ϕ_{21} along with the lengths of ϕ_1 and ϕ_2 is approximately the time available to latch a signal. This interval is kept constant at a lower operational speed and the test is performed again. The results do not change providing confirmation of the proposed explanation of the failure.

2.2. Tap Design Issues

All CAZM simulations showed an appreciable delay through the test access points. A block diagram of a tap is provided in Figure 13 of WUCS-89-52. The multiplexor on the input side does not give any extra drive, and the signal entering a tap has to charge

the capacitance associated with all three inverter cells connected to the output node of the multiplexor. This causes an appreciable delay which given the results from device testing of PP3 calls for redesign.

3. BTT Redesign

The BTT was unable to latch incoming data at high speed because the shift registers at the end of the interface regenerated the signal with respect to the clock. The *mil* latch signal was buffered by a large driver which delayed it so that it arrived while data was changing. Figure 4 shows a block diagram of how the latching signals for the BTT were set up. The most robust solution to reducing the delay experienced by signals such as *mil*, *lat* and *ld* is to qualify them with unbuffered $\phi 1$ instead of buffered $\phi 1$ because that reduces about 5 ns from the delay which satisfies the required constraints. A *CAZM* simulation showed that after the change *mil* did not overlap with the following $\phi 2$ any more at the simulation speed of 42MHz.

A block diagram of the downstream portion of the BTT in version 1. of the BTC appears in Figure 5.

This shows that the *PISO* shift registers are qualified by an ordinary clock. The signal *ld* is qualified by a $\phi 1$ and it appears that the output node of the downstream *PISO* latches are driven not only by the latches, but also by the preceding stage. This would cause a set of unresolved nodes. The chip did not exhibit an error because of the skew between the signals but with the modified *ld* this would cause a problem. Thus, a new signal was created called *ldop* that would be asserted during $\phi 1$ except during the clock cycle that *ld* was asserted. This signal was used in place of $\phi 1$ in the same configuration that appears in Figure 5. Figure 6 shows the relationship between *ld*, *ldop* and the clocks.

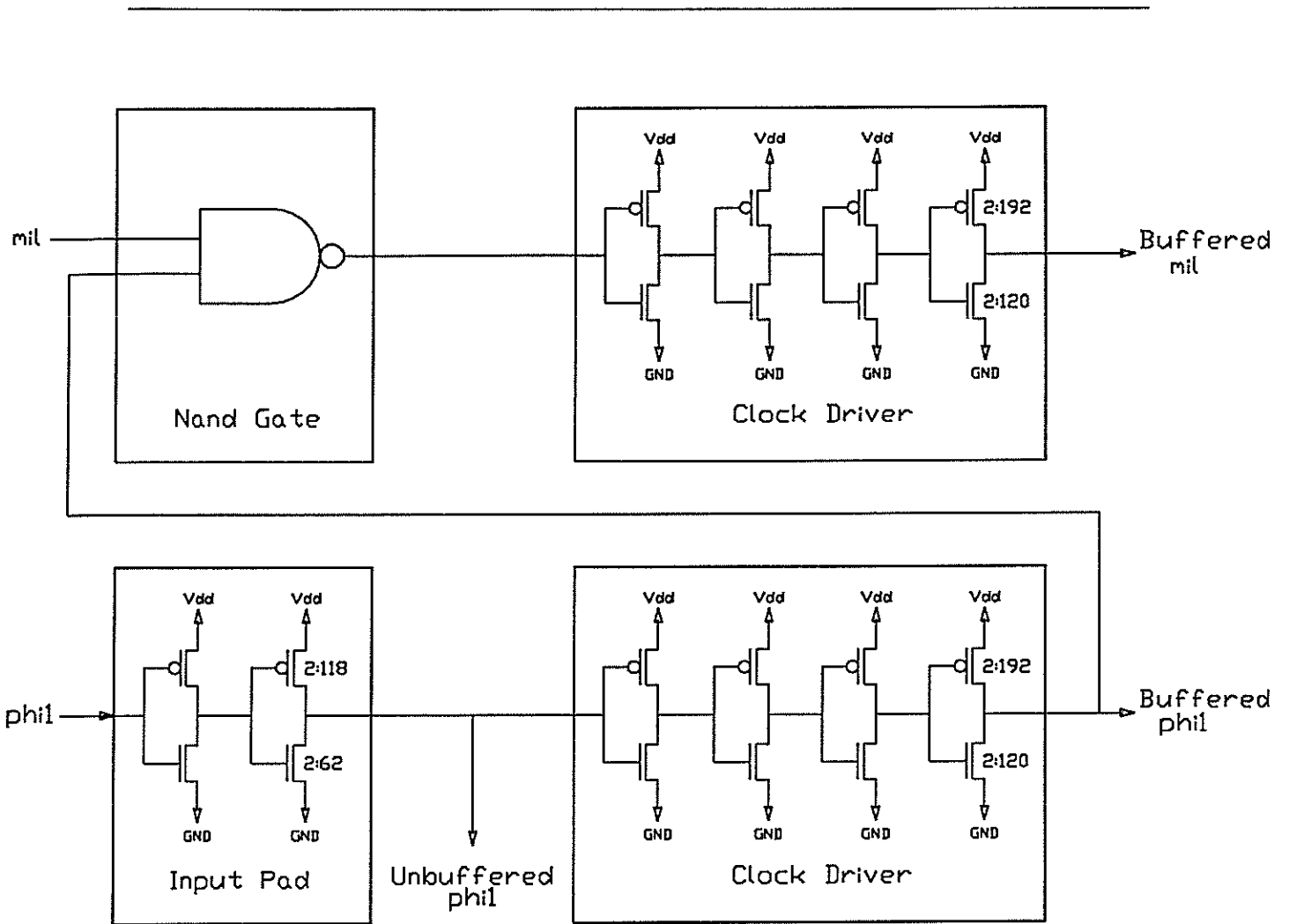


Figure 4. Block Diagram of BTT Latching Signals

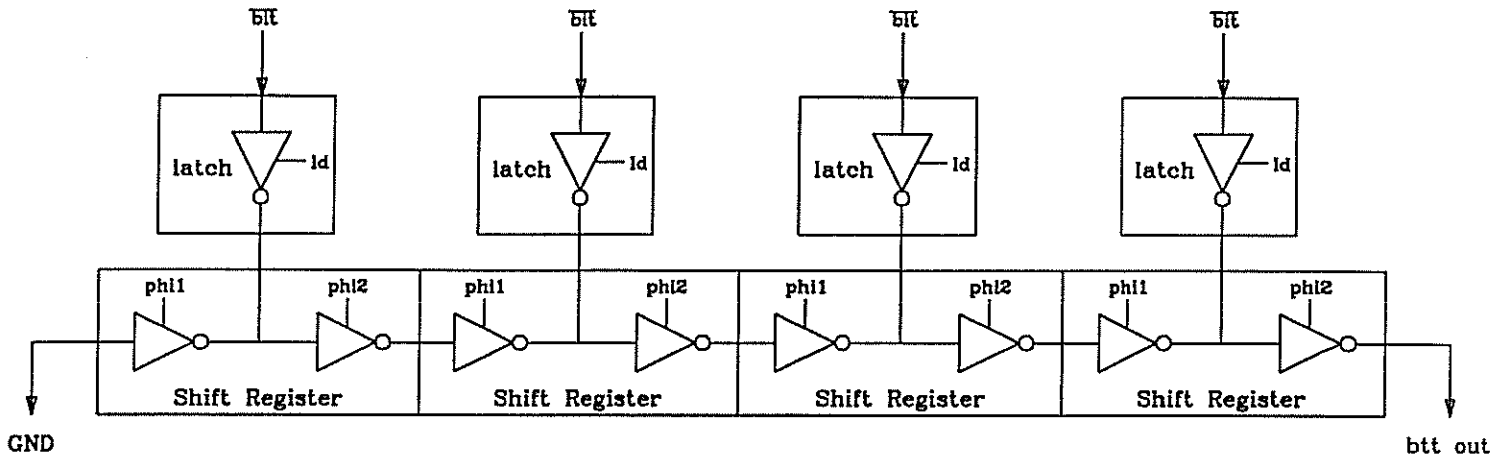


Figure 5. BTT Output Circuitry

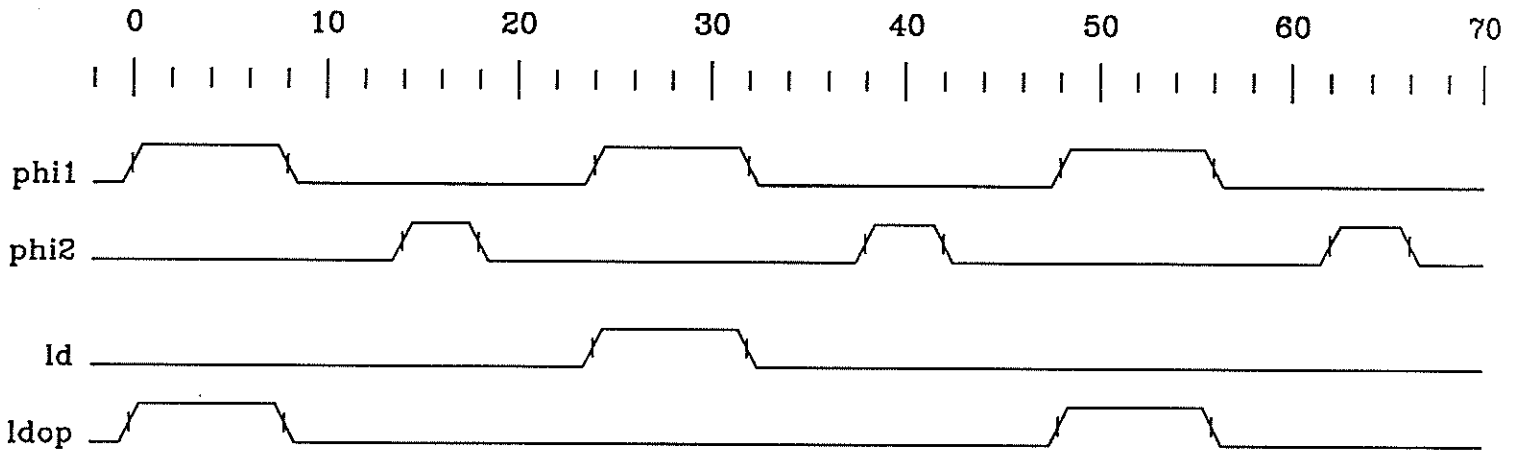


Figure 6. Relationship of ld, ldop, and clocks

4. BTT Input Interface

All inputs to the BTT were changed to be buffered by an extra clock cycle via a set of 1-bit shift registers. This includes the *pt* signal, the addresses to the BTT and the data

path. The shift registers were placed as close to the output from the *INC* as possible and the register clocking the *pr* signal was physically located just before the first tap on the line. All of this resulted in a more robust design where all the signals appeared to have better timing tolerances.

5. Tap Design

As mentioned before the original tap design was found to be inadequate. A new design was suggested that would remove the function that allowed the user to put data from the pins directly onto an internal bus. The circuitry associated with a single line passing through a test access point is shown in Figure 7. It has the nice property that all internal nodes of the tap are driven from within the tap itself.

This design change also resulted in replacement of all bidirectional pads on the chip by output pads, in removal of all the multiplexer arrangements dealing with bidirectional signals, and in removal of the direction signals controlling the three test buses.

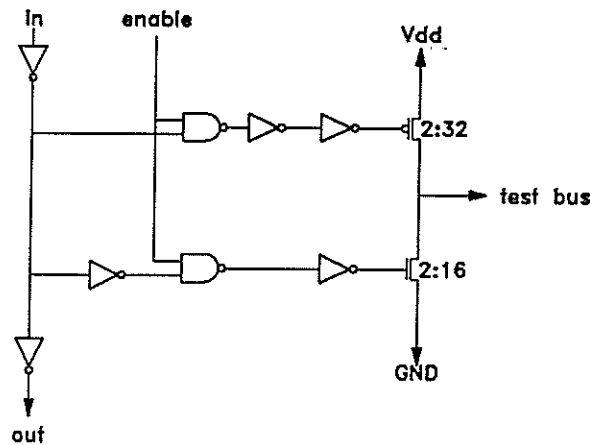


Figure 7. New Tap Design
