Report Number: WUCS-90-08

1990-05-01

VLSI Area Comparison of Benes and Crossbar Communications Networks

Authors: Tony Y. Mazraani

A high-level area model of Benes and crossbar networks in a VLSI environment is presented. The areas of both networks are then compared for different design parameters. The results are also compared to those obtained by Franklin [Fr81] for banyan and crossbar networks. The geometric chip layout employs two metal layers for the interconnection paths. It is show that both Benes and crossbar grow in area as O(N)2, where N is the network size.

VLSI AREA COMPARISON OF BENES AND CROSSBAR COMMUNICATIONS NETWORKS

Tony Y. Mazraani

WUCS-90-08

May 1990

Department of Computer Science
Washington University
Campus Box 1045
One Brookings Drive
Saint Louis, MO 63130-4899

Abstract

A high-level area model of Benes and crossbar networks in a VLSI environment is presented. The areas of both networks are then compared for different design parameters. The results are also compared to those obtained by Franklin [Fr81] for banyan and crossbar networks. The geometric chip layout employs two metal layers for the interconnection paths. It is shown that both Benes and crossbar grow in area as $O(N^2)$, where N is the network size.

VLSI AREA COMPARISON OF BENES AND CROSSBAR COMMUNICATIONS NETWORKS

Tony Y. Mazraani

1. INTRODUCTION

The rapid developments in VLSI technology over the last few years have prompted the research community as well as the computer industry to use VLSI techniques for building massively parallel multiprocessors with hundreds or even thousands of processors. Using VLSI technology for such complex systems is very challenging. Problems that should be taken into account include chip layout of switch nodes and links, chip area and delay analysis, and clock synchronization.

Two parameters, area and delay, are usually used as performance criteria. This paper is concerned with two network types: crossbar [Pi75] and Benes [Be65]. It compares the areas of both networks in a VLSI environment, where it is assumed that the entire interconnection network resides on a single VLSI chip. Both networks are assumed to operate in a circuit switched mode.

First, an introduction to both crossbar and Benes networks is presented in section 2. The third section presents area models developed for both networks and comparisons of Benes/crossbar area requirements. The final section contains the conclusions of the paper.

2. REVIEW OF CROSSBAR AND BENES NETWORKS

The overall structure and switch positions of crossbar and Benes networks of size $N = 8$ (eight input/eight output ports) are depicted in Figures 1 and 2. The P and M notation represents processor and memory.

Both networks have full interconnection capabilities; it is possible to set up a connection from any input port to any output port as long as the switches are in the proper positions. Each switch can control its position thus allowing self-routing of

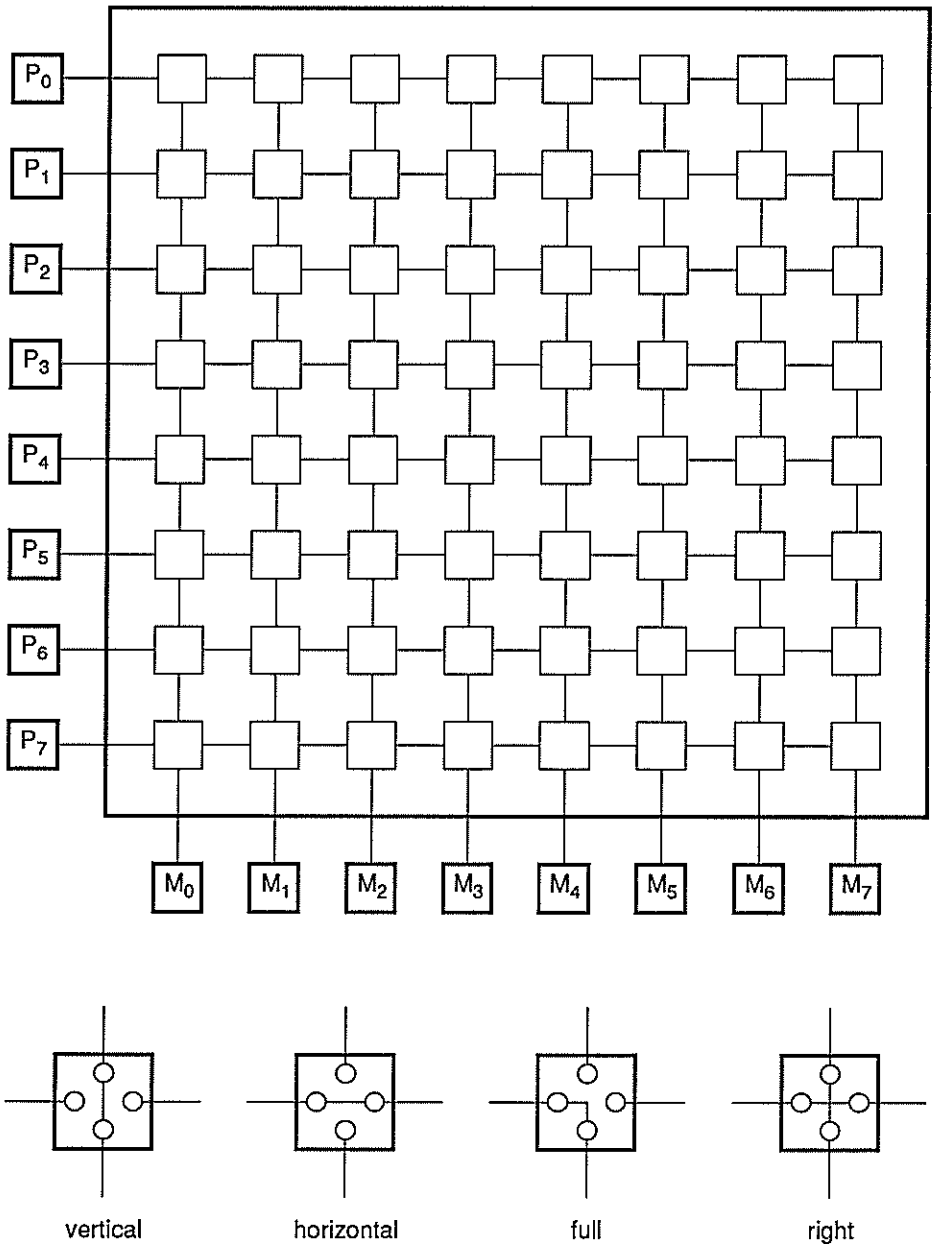

Figure 1: 8×8 crossbar network with possible switch positions

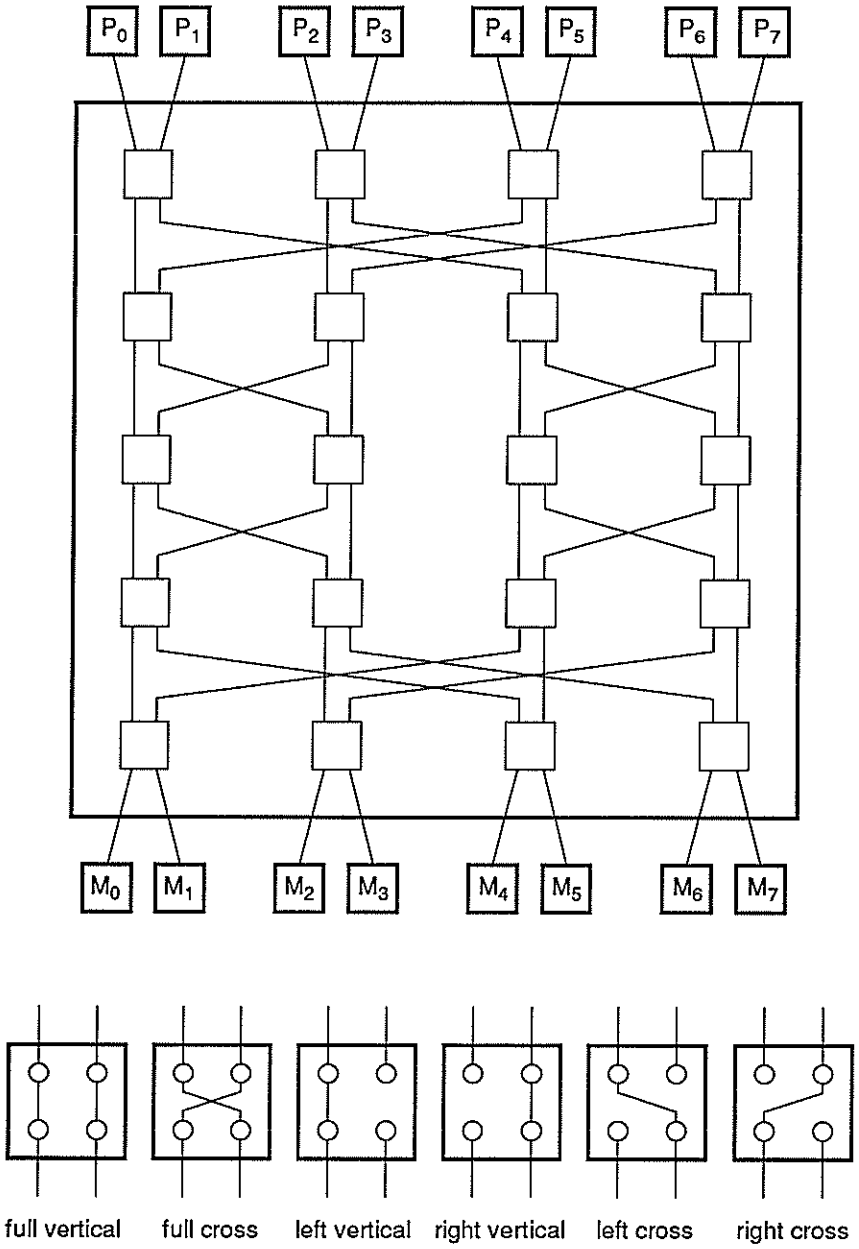

Figure 2: 8×8 Benes network with possible switch positions

messages through the system. In the crossbar network, no blocking occurs as long as each input port requests a connection to a unique output port. In this case, all messages can be routed through the network concurrently. In Benes network, it is possible that two messages or connections destined for two different output ports will require use of the same communication path between switches. This results in blocking of messages, bandwidth reduction, and delays in the network. The blocking probability for Benes networks versus network size is illustrated in Figure 3 [Pi75]. The network is assumed to operate in a circuit switching mode. More details on blocking probability may be found in [Me88] and [Va90].

3. VLSI AREA MODEL

In order to compare the VLSI area of Benes and crossbar networks, certain assumptions must be made and general parameters defined. These are design as well as technology related. The objective is to develop equations for the area taken by a single switch and then apply them to both Benes and crossbar networks.

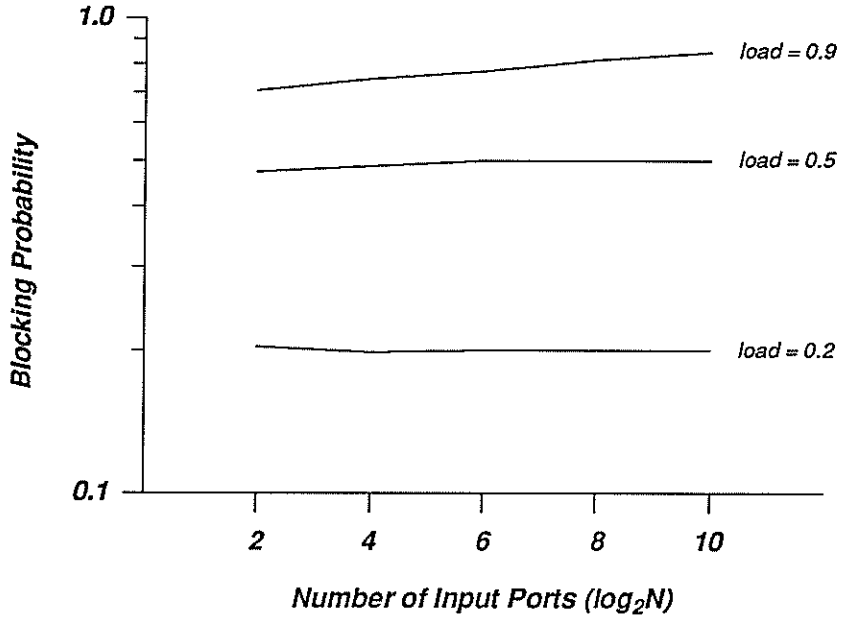

Figure 3: Blocking probability for Benes network vs. network size using 2×2 switches

As far as the area is concerned, on can think of a Benes network as being equivalent to two banyan networks connected in the fashion shown in Figure 4. Hence, the area model presented in this paper follows from the model developed by Franklin [Fr81] for banyan and crossbar networks. In this paper, we have extended the model to apply to Benes network and incorporate changes for current CMOS technology.

The geometric shape of the individual switches which make up the network are very difficult to describe exactly. They consist of a group of individual blocks connected together in a specified manner. However, in this analysis, we assume that the shape of each switch is a square of area A and side length L. Furthermore, because of the assumption of comparable switch complexity in Benes and crossbar networks, all switches are taken to be of equal size.

A particular switch can be roughly divided into two parts: one part is associated with data paths and occupies area A_d, while the other is associated with control of these data paths and occupies an area A_c. The area of the data portion is chiefly dependent on the data path width which is denoted by w. The control portion is assumed to be independent of the path width.

Two design parameters can now be defined. The first one, denoted by γ, is the ratio of A_c to A_d given a path width equal to one.

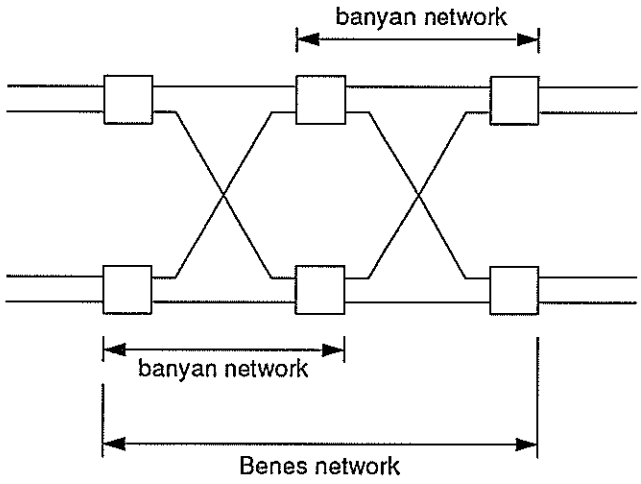

Figure 4: Comparison of Benes and banyan network structures

$$\gamma = \left.\frac{A_c}{A_d}\right|_{w=1} \tag{1}$$

The second parameter K is defined as the ratio of A_d to the minimum area required given a path width equal to one. This minimum area is a function of the feature size λ which depends on the particular technology and fabrication process used ($\lambda = 1$ micron for typical current commercial processes). Current CMOS technology recommends a minimum line width and minimum distance between adjacent lines of 3λ each for metal layer one denoted by M_1. Therefore, the width of a path containing w parallel communications lines would be

$$3w + 3(w-1) = 6w - 3 \cong 6w \text{ for large } w.$$

Assuming each switch side has w communications lines, a lower bound on the area of the data portion is $(6w)^2$. Hence, K can now be defined as

$$K = \frac{A_d}{(6w)^2} \text{ where } (K \geq 1). \tag{2}$$

For $w = 1$ and from (1) we get $A_c = A_d\gamma = 36K\gamma$. We can therefore obtain an expression for the switch area in terms of the parameters γ, w, and K.

$$A = A_c + A_d = 36K(\gamma + w^2)$$

The side length L of a switch is therefore

$$L = \sqrt{A} = 6\sqrt{K(\gamma + w^2)} \tag{3}$$

The equations developed for K and L are employed in deriving the area model for Benes and crossbar networks.

3.1. Crossbar Area Model

A small portion of larger crossbar network is depicted in Figure 5. Assuming that the network has a square area with N input and N output ports, then the side length denoted by L_s can be expressed as

$$L_s = NL + 3(N-1)$$

The area required by the crossbar network is therefore

$$A_{CB} \cong L_s^2 = [NL + 3(N-1)]^2 \tag{4}$$

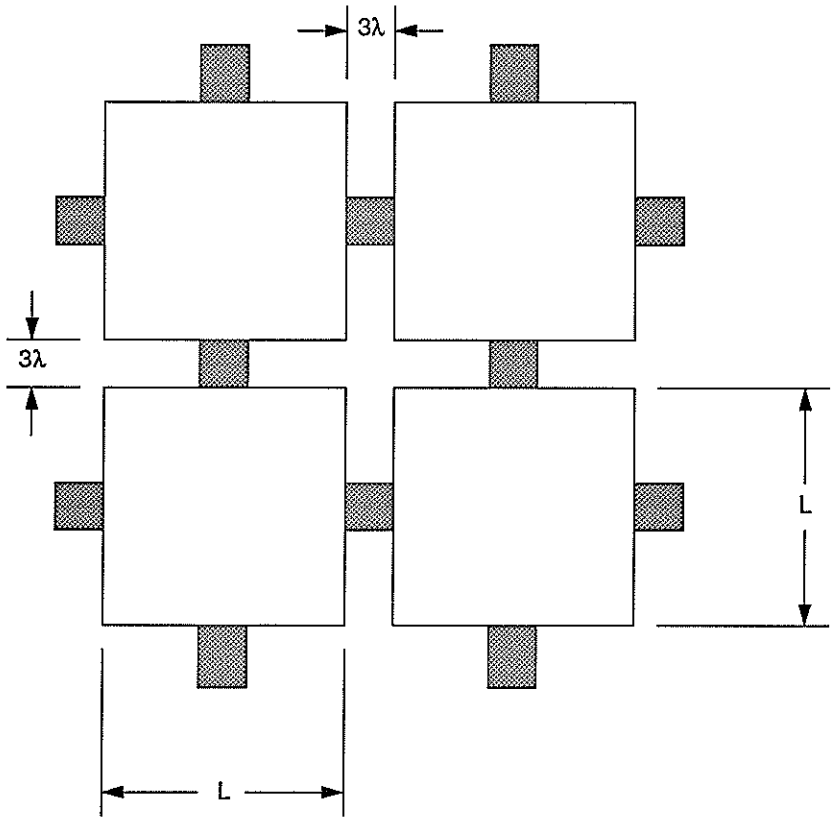

Figure 5: Portion of a larger crossbar network

Substituting for L from (3) in (4) we obtains

$$A_{CB} \cong \left[6N\sqrt{K(\gamma+w^2)} + 3(N-1)\right]^2 \tag{5}$$

3.2. Benes Area Model

The Benes VLSI area model follows from the banyan VLSI model derived by Franklin. The model employs two layers of metal interconnects denoted by M_1 and M_2 which provide for all horizontal and vertical paths, respectively. Unlike the minimum width used for vertical paths by Franklin, current technology [Mo87] recommends a minimum M_2 line width of 4λ. This change is irrelevant in the case of crossbar area model because metal interconnects do not crossover. That is, a single M_1 layer is sufficient for horizontal and vertical paths.

The layout used in determining the horizontal length of a Benes network is illustrated in Figure 6. The advantage of this layout is that it produces the minimum horizontal length. The only drawback is that the switch side length should be greater than the vertical spacing occupied by the $2w$ lines between the two switches.

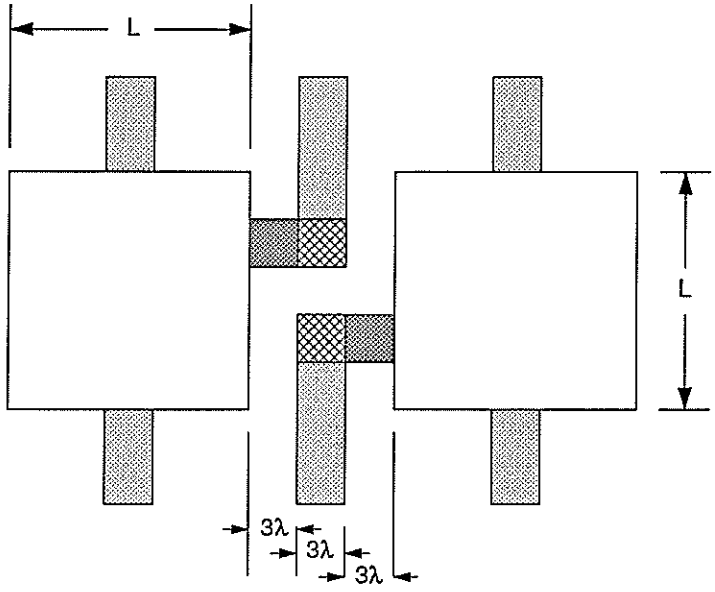

Figure 6: Minimum layout geometry for Benes network

Given a network of size N, the horizontal length occupied by all switches is $(N/2)L$. The minimum horizontal spacing taken by the interconnect paths is given by

$$L_h = 4\left(\frac{N}{2}-1\right)(2w-1)+2\times 3\left(\frac{N}{2}-1\right)$$

$$= \left(\frac{N}{2}-1\right)[4(2w-1)+6]$$

The minimum horizontal length of the whole Benes network can therefore be written as follows

$$L_{BEH} = \left(\frac{N}{2}\right)L + L_h$$

$$= \left(\frac{N}{2}\right)L + \left(\frac{N}{2}-1\right)[4(2w-1)+6] \qquad (6)$$

The vertical length is more difficult to derive because unlike the horizontal length, the distances between switch rows increase as one moves from the center switch row to the input and output ports of the network. The reason for this is that as the number of path crossovers increase, the distance between switch rows increases accordingly. This distance results from the fact that for each additional interconnect path of width w, the level-to-level vertical length increases by roughly $6w$.

The network level numbering scheme used in this analysis is as follows (refer to Figure 2). Assuming that the center switch row is the reference row, then all levels above that are numbered as level 1, 2, 3, etc.; all levels below that are numbered as level –1, –2, –3, etc. The minimum vertical distance between switch rows at levels 1 and –1 is 3 as shown in Figure 7. For higher levels, the vertical distance is a function of the network size N and the path width w. A minimum layout geometry for level 2 is illustrated in Figure 8. This layout assumes a path width w equal to one and includes only paths with horizontal components. The total level-to-level vertical length can therefore be expressed as follows

$$L_{BEVL} = 2\left(3+\sum_{i=2}^{\left\lceil \log\left(\frac{N}{2}\right)\right\rceil} 3n_i\right) \qquad (7)$$

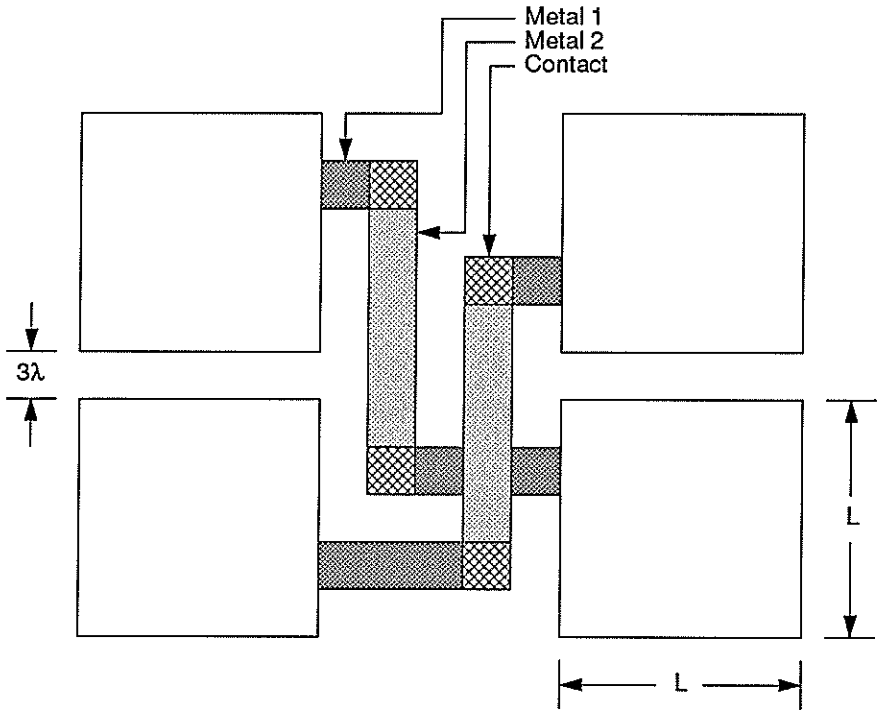

Figure 7: Minimum vertical distance for levels 1 and –1

where

$$n_i = 2(2^i - 1)w + 1$$

is the number of horizontal paths at level i.

The overall vertical length of the network is the sum of three vertical lengths: the level-to-level length derived in (7), the length (L) of the individual switches, and the length associated with the drivers which drive the lines from level to level. The drivers design approach used here follows from [Co80]. This approach is concerned with minimizing the delay associated with driving level-to-level lines by using a chain of drivers where the final driver stage is matched in area to the load it is driving. The area in this design, however, increases from level to level.

In order to derive an expression for the area taken by the drivers, we introduce two types of paths (see Figure 9): type 1 path which is purely vertical with length p_{i1}

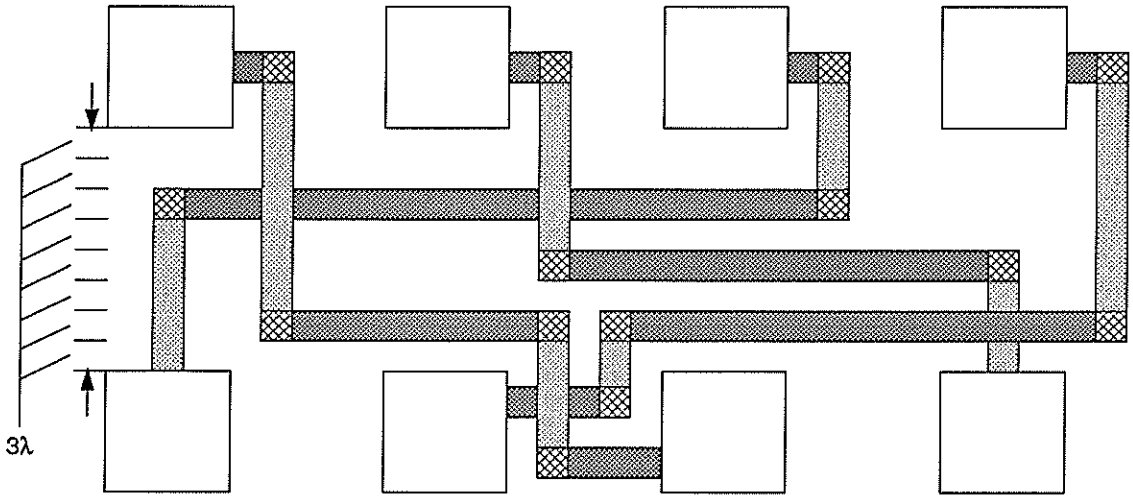

Figure 8: Level 2 minimum vertical layout geometry

and type 2 path with length p_{i2} which has both horizontal and vertical lengths. As shown in Figure 9, p_{i1} depends mainly on the level-to-level vertical length. Therefore, it can written as follows:

$$p_{i1} = \begin{cases} 3n_i & \text{for i} > 1 \\ 3 & \text{for i} = 1 \end{cases} \tag{8}$$

The length of the vertical component in the type 2 path is roughly equal to $p_{i1} + L/2$. The lengths that contribute to the length of the horizontal component are shown in Figure 9. The overall type 2 length can thus be expressed as

$$p_{i2} = (2^{i-1}-1)L + 2^{i-1}[4(2w+1) + 2\times 3] + \frac{L}{2} + p_{i1} + \frac{L}{2} \tag{9}$$

Let p_{i2V} and p_{i2H} be the vertical and horizontal lengths of p_{i2}, respectively. Therefore,

$$p_{i2V} = p_{i1} + \frac{L}{2}$$

and

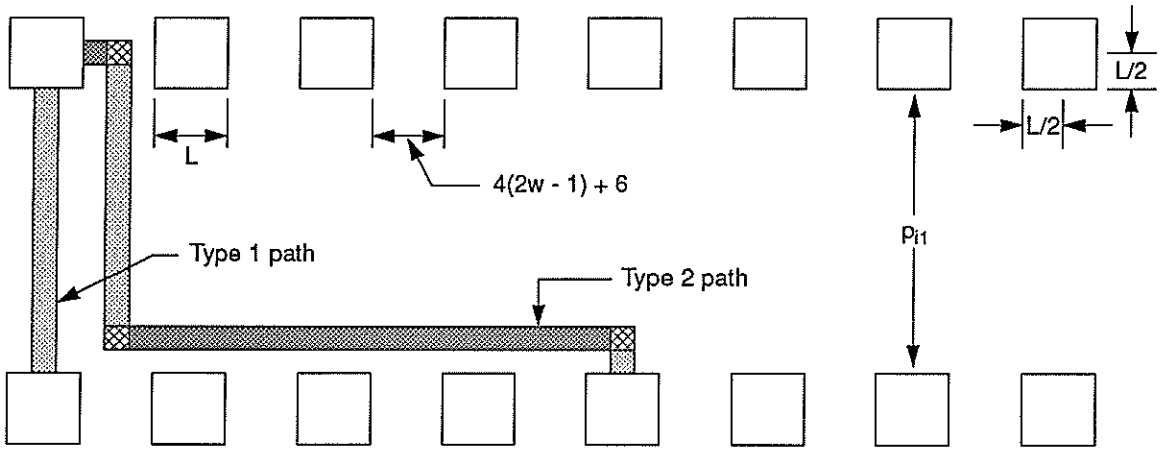

Figure 9: Type 1 and type 2 paths at network level 3

$$p_{i2H} = (2^{i-1}-1)L + 2^{i-1}[4(2w-1)+2\times 3] + \frac{L}{2}$$

For a switch at level i with a path width w, the total area occupied by type 1 and type 2 paths is given by

$$A_{PATH} = 4w(p_{i1} + p_{i2V}) + 3wp_{i2H} \tag{10}$$

The first term above represents the area taken by the vertical communications paths which use M_2 layer (with minimum width of 4λ per line). The second term is the area taken by the horizontal paths which use M_1 layer (with minimum width of 3λ per line). Taking the design approach of [Co80] into account, the overall driver area can be estimated as follows:

$$A_{DRIVER} = 4wv_2(p_{i1} + p_{i2V}) + 3wv_1p_{i2H} \tag{11}$$

where v_1 and v_2 correspond to the ratio of the driver's area to M_1 and M_2 line areas, respectively. Lower bounds on the parameters v_1 and v_2 are 0.0357 and 0.0179, respectively (see Appendix). Assuming that the layout of drivers increases the switch

area only in the vertical size, then the area contribution in the vertical direction is given by A_{DRIVER}/L. The overall vertical length contributed by the drivers and switches is therefore

$$L_{BEVS} = 2\sum_{i=1}^{\lceil \log N \rceil}\left\{\frac{4wv_2}{L}(p_{i1}+p_{i2V})+\frac{3wv_1}{L}p_{i2H}+L\right\}-L \tag{12}$$

The last term in (12) is needed because of the symmetry of Benes network with respect to the center switch row. That is, the vertical distance L of the center switch row contributes twice to L_{BEVS} in the first term of (12).

The overall vertical length for a Benes network is thus the sum of (7) and (12) and is given by

$$L_{BEV} = L_{BEVL}+L_{BEVS} \tag{13}$$

The Benes area is thus

$$A_{BE} = L_{BEH}L_{BEV} \tag{14}$$

4. BENES/CROSSBAR AREA COMPARISONS

The ratio of A_{BE}/A_{CB} is used to compare the VLSI area requirements for both networks. It is expressed as a function of the design parameters γ, K, w, v_1, v_2, and N. Figure 10 shows this ratio as a function of the network size N and the path width w. The other design parameters are set to the same values used in the model derived by Franklin. Notice that the area of Benes network increases as the path width increases. The reason for this is that for higher path widths, the number of crossover paths increases thus increasing the level-to-level area.

In Figure 11, the design parameters v_1 and v_2 are doubled. Notice that the area of Benes network is larger than the previous case for all w. This is to be expected since doubling v_1 and v_2 means that larger driver area is now required for driving the lines from level to level.

The design parameter K is then doubled as depicted in Figure 12. This means that the increased area in A_d over the minimum required to support a w wide path is doubled. In this case, we notice that for high path widths, the ratio is close to one. Hence, the areas taken by Benes and crossbar networks are roughly the same. Figure 13 shows all three cases presented above.

The results depicted in Figure 10 are then compared to those obtained by Franklin (see Figure 14). The area of Benes network is roughly double that of banyan network. This is to be expected since Benes network is equivalent to a two banyan networks when connected in the fashion shown in Figure 4. Note that the design parameters v_1 and v_2 are introduced in the new model to account for the use of M_2 metal layer.

5. CONCLUSIONS

This paper has presented area models and comparisons of crossbar and Benes networks in a VLSI environment. The geometric chip layout employs two metal layers, M_1 and M_2, for the communications paths. The parameters used in deriving the drivers area are based on a CMOS implementation. Both networks are shown to grow in area as $O(N^2)$, where N is the switch size.

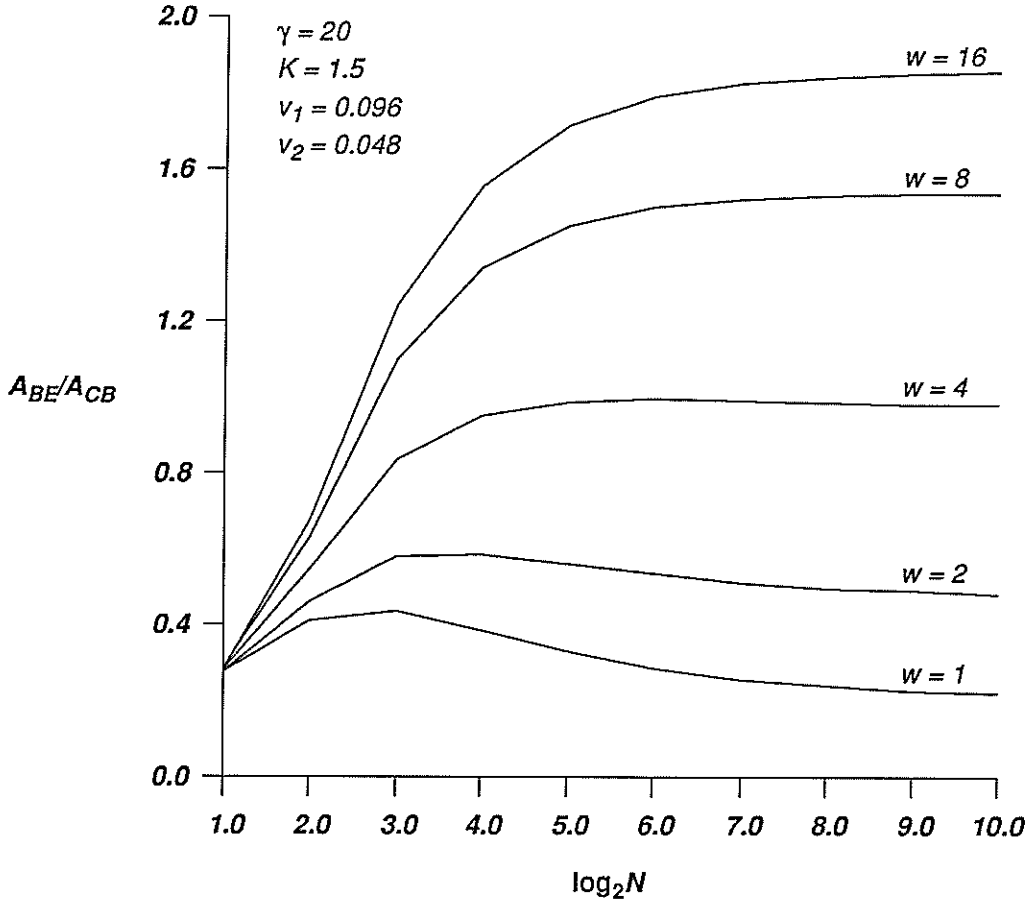

Figure 10: Ratio of Benes to crossbar area requirements

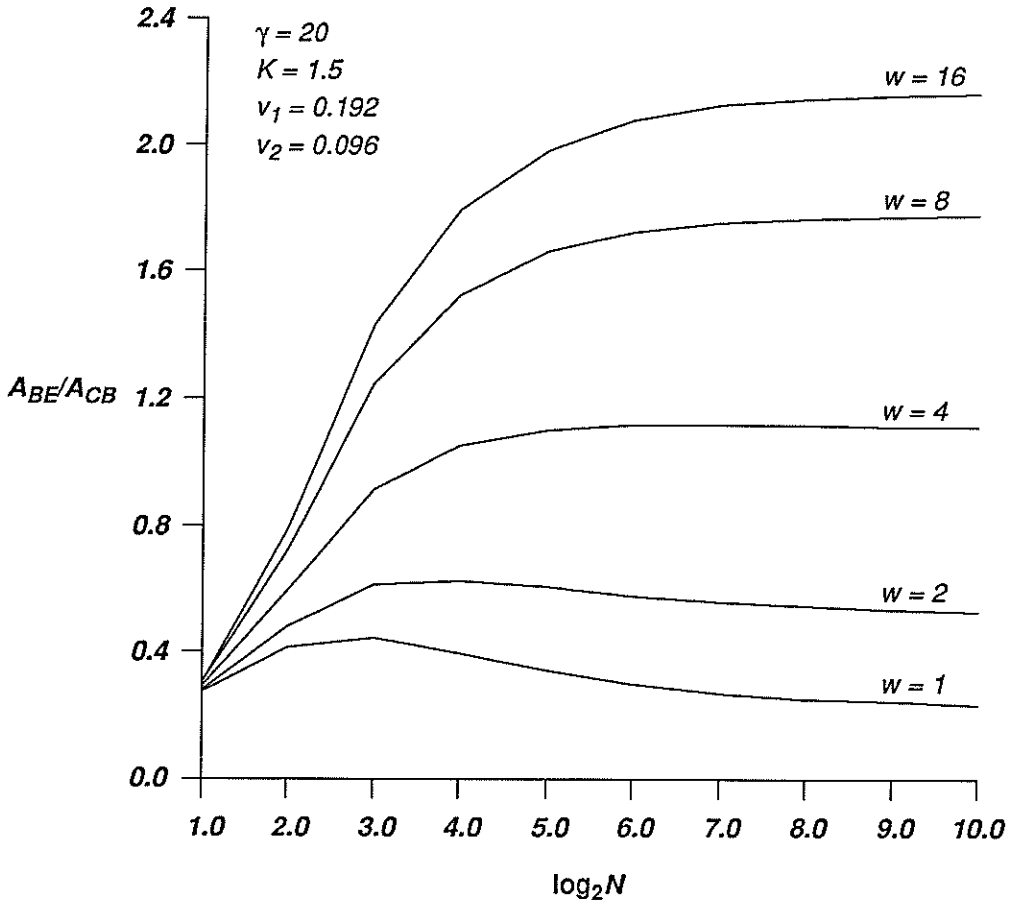

Figure 11: Ratio of Benes to crossbar area requirements (v_1 and v_2 doubled)

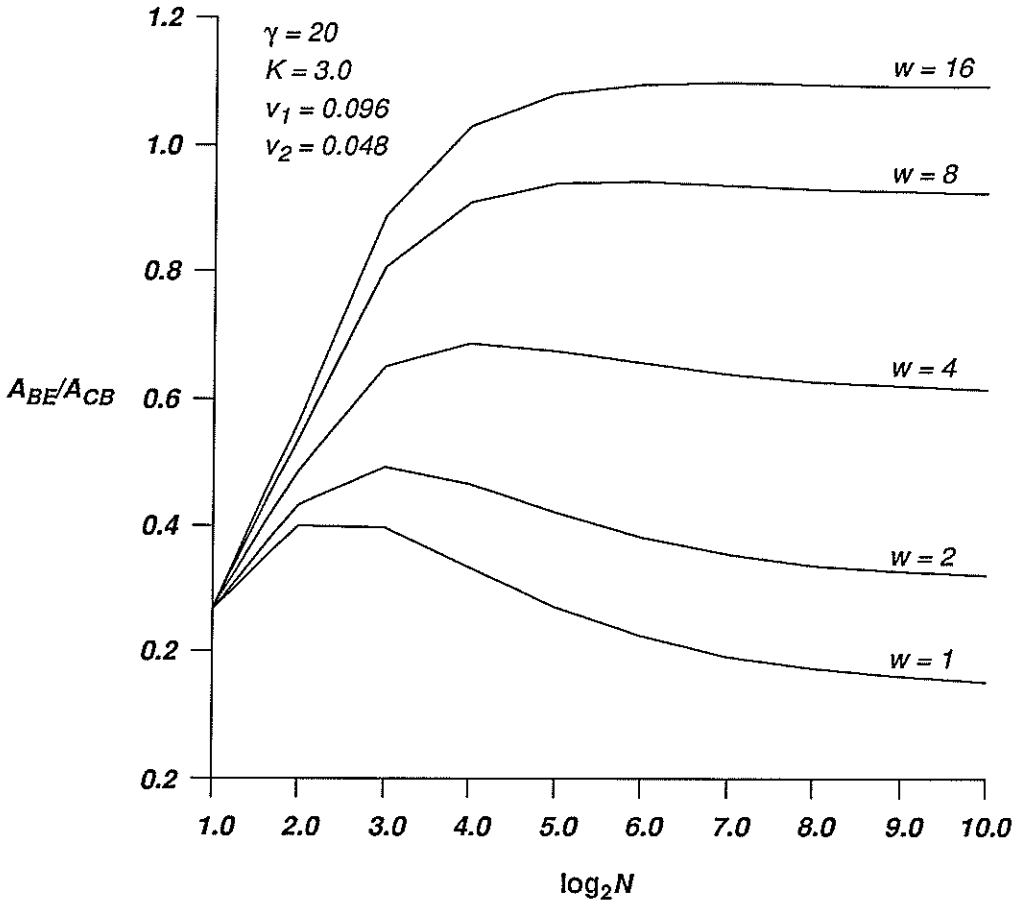

Figure 12: Ratio of Benes to crossbar area requirements (K doubled)

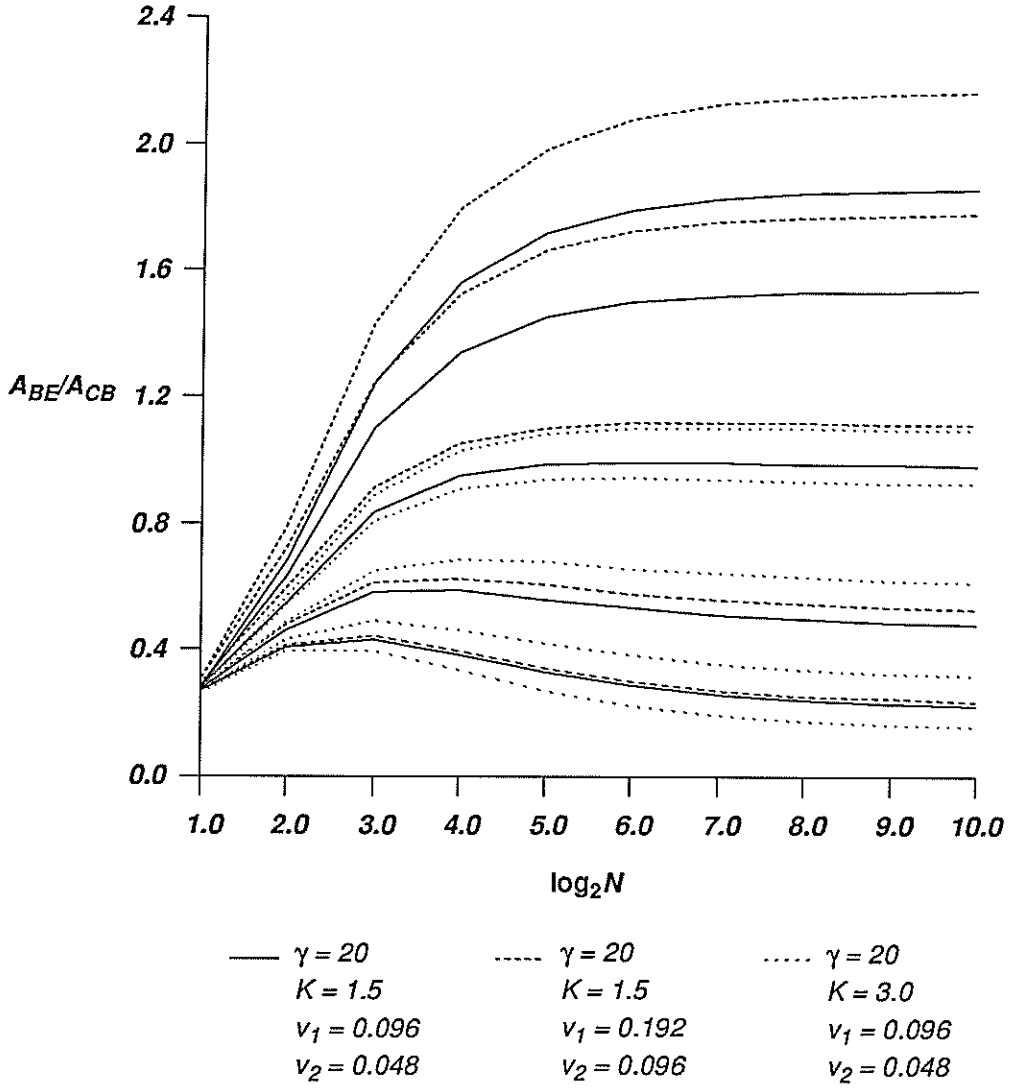

Figure 13: Ratio of Benes to crossbar requirements for different design parameters

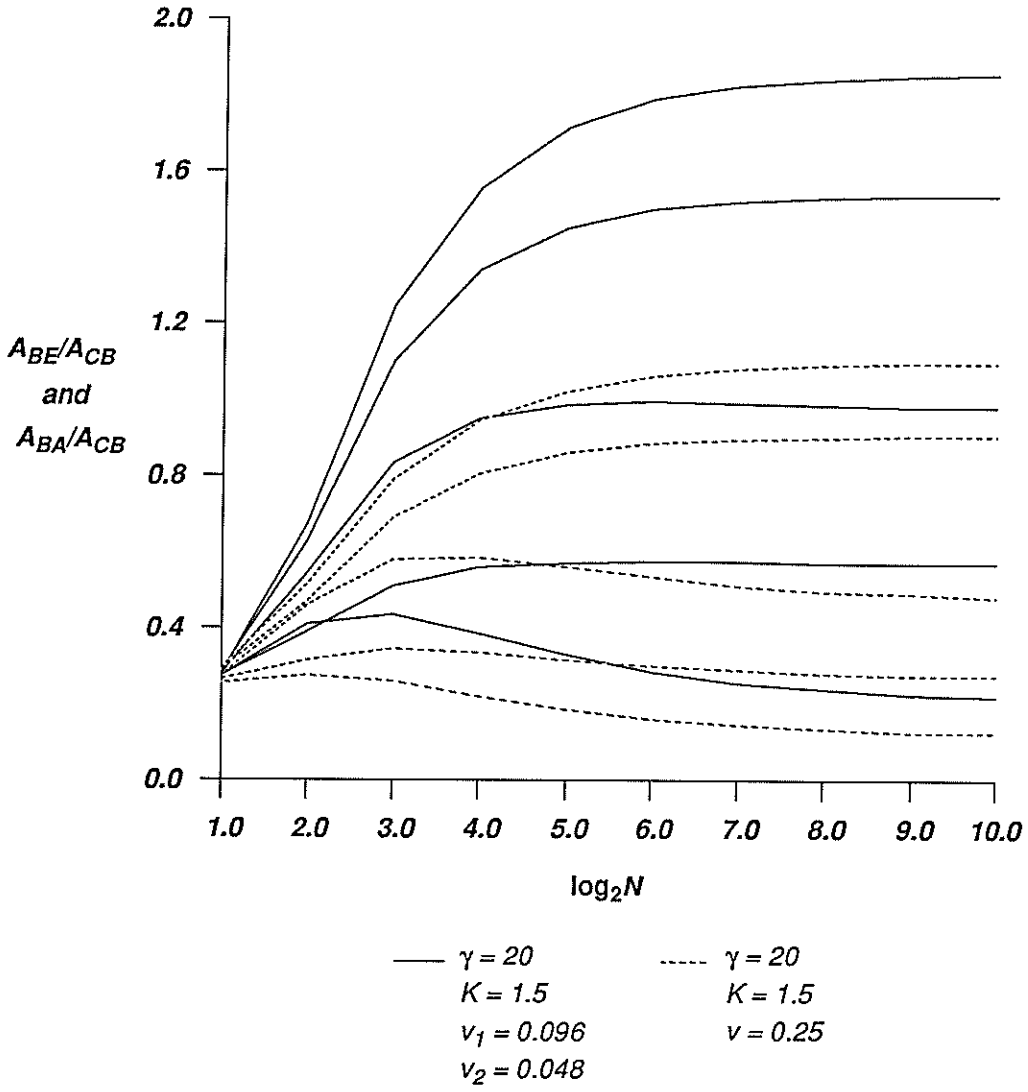

Figure 14: Comparison of Benes/crossbar and banyan/crossbar area requirements

APPENDIX

A. Lower Bounds on Line Driver Area

Following the delay analysis of an inverter chain developed by Mead and Conway [Co80], assume a chain of K inverters are present. Each inverter in the chain is larger than the previous one by a factor of g. The (K – 1)st inverter drives a line whose capacitance is C_L. The minimum size inverter has a gate capacitance C_G. Assuming g has been selected so that $g^K = C_L/C_G$, then a lower bound on the area of the inverters would be

$$A_{DRIVER} > A_{MIN}(1 + g + g^2 + \ldots + g^{K-1}) = A_{MIN}\sum_{i=0}^{K-1} g^i$$

Hence,

$$A_{DRIVER} > A_{MIN}\frac{(g^K - 1)}{(g-1)} = A_{MIN}\frac{(A_L/A_{MIN})\,(C_L/C_G) - 1}{(g-1)}$$

where A_L is the area of the line to be driven. Given the current technology parameters [Ro87],

$$(C_L/C_G)_{M1} \approx 0.0357$$
$$(C_L/C_G)_{M2} \approx 0.0179$$

where M_1 and M_2 correspond to metal 1 and metal 2 layers, respectively.

The optimum g (*i.e.*, g for which the delay through the chain of inverters is minimum) can be determined by plotting the total delay for different values of g. This delay is given by

$$d_g = \alpha\frac{g}{ln\,(g)}$$

where α is a constant. The multiplicative factor, $g/\ln(g)$, is plotted as a function of g in Figure 15, normalized to its minimum value (e). The minimum delay is obtained for

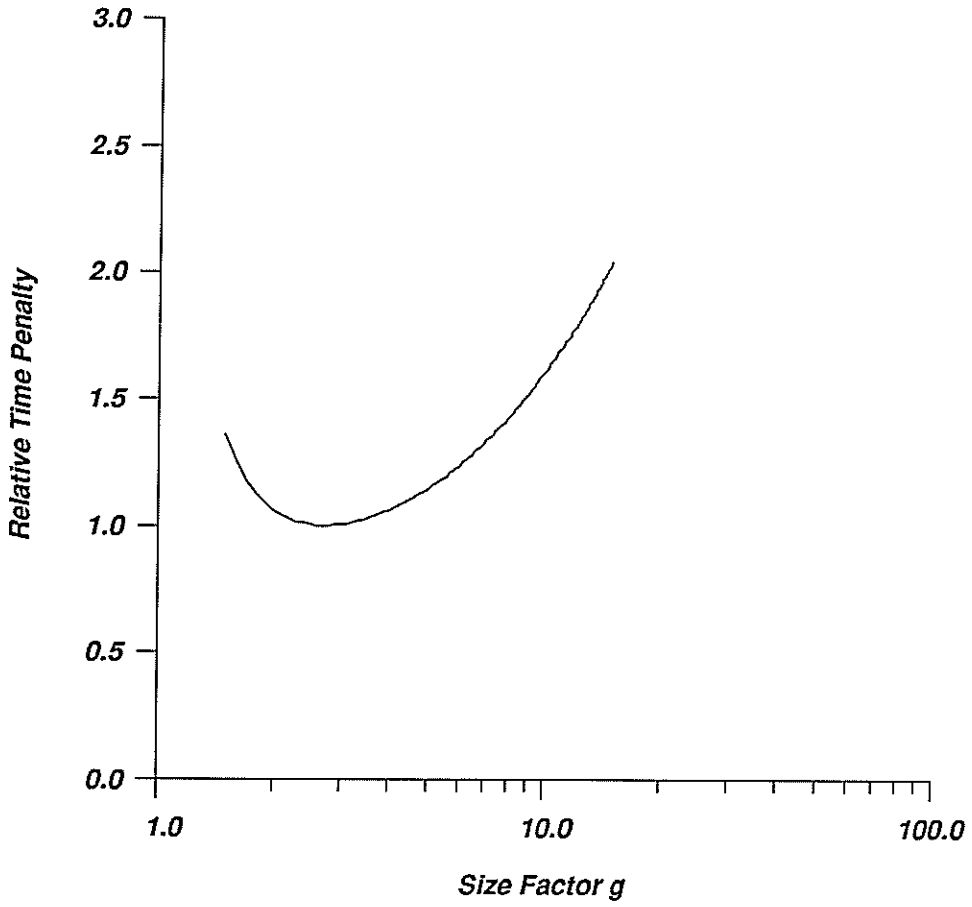

Figure 15: Delay versus size factor g

$g = 2.80$. Therefore, for long metal lines,

$$A_{DRIVER} > A_L/78.43 \text{ for M1} \Rightarrow v_1 = 1/78.43 = 0.0128$$

and

$$A_{DRIVER} > A_L/156.42 \text{ for M2} \Rightarrow v_2 = 1/156.42 = 0.0064$$

It is important to note here that this analysis does not take into account any area needed due to pull-up transistors; nor does it take into account any area needed due to layout constraints.

B. Computer Program for Computation of Areas

The statistics presented in this paper were computed using the *C*-program shown below. This program computes A_{BE}, A_{CB}, and the ratio A_{BE}/A_{CB} for different values of w, N, γ, K, v_1, and v_2. All results are stored in a file called `ratio.dat`.

```
#include <stdio.h>
#include <math.h>

#define     v1   0.096 /* ratio of driver's area to M1 line area */
#define     v2   0.048 /* ratio of driver's area to M2 line area */
#define     log2(n)   log(n)/log(2.) /* define macro for log base 2 */

FILE        *outfile; /* output file where results are stored */


main()
{
    double      gamma, /* ratio of control to data areas */
                K, /* increased area in Ad */
                L, /* length of switch side */
                LBEH, /* minimum horizontal lengths */
                LBEVL, /* total level-to-level length */
                LBEVS, /* vertical contribution of switches */
                LBEV, /* overall vertical length */
                ACB, /* crossbar switch area */
                ABE, /* Benes switch area */
                sum = 0.0, /* dummy variable used for summation */
                w, /* data path width */
                N, /* switch size */
                ratio, /* ratio of Benes to crossbar area */
                sumlimit1, /* upper limit on a sum */
                sumlimit2, /* upper limit on a sum */
                i; /* dummy variable */

    /* read input parameters */
    printf("gamma = ");
    scanf("%F", &gamma);
    printf("K = ");
    scanf("%F", &K);

    /* open outfile for storing results */
    outfile = fopen("ratio.dat","w");
```

```
        for(w=1.;w<=16.;w=w*2.){ /* scan over all values of w */
            for(N=2.;N<=1024.;N=N*2.){ /* scan over all values of N*/
                /* compute upper limit of sums */
                sumlimit1 = ceil(log2(N/2.));
                sumlimit2 = ceil(log2(N));

                /* side length of switch */
                L = 6.*sqrt(K*(gamma + pow(w,2.)));

                /* crossbar switch area */
                ACB = pow((N*L + 3.*(N - 1.)),2.);

                /* compute Benes switch area */
                LBEH = (N/2.)*L + (N/2. - 1.)*(8.*w + 2.);
                sum = 0.0;
                if (sumlimit1 >= 2.){
                    for(i=2.;i<=sumlimit1;i++)
                        sum = sum + (6.*w*(pow(2.,i) - 1.) + 3.);
                }
                LBEVL = sum + 3.;
                sum = 0.0;
                if (sumlimit2 >= 2.){
                    for(i=2.;i<=sumlimit2;i++)
                        sum = sum + (4.*v2*w*(12.*w*(pow(2.,i) - 1.)
                        + 6. + L/2.)
                        + 3.*v1*w*(((pow(2.,(i-1.))) - 1.)*L
                        + (pow(2.,(i-1.)))*(8.*w + 2.)))/L
                        + L;
                }
                LBEVS = sum + (4.*v2*w*(6. + L/2.) + 3.*v1*w*(8.*w + 2.))/L + L;
                LBEV = 2.*LBEVL + 2.*LBEVS - L;

                /* Benes switch area */
                ABE = LBEH * LBEV;

                /* ratio of Benes to crossbar area */
                ratio = ABE/ACB;

                /* store result in output file */
                fprintf(outfile," %3.1f\t%6.4f\n", log2(N), ratio);
            }
        }
        fclose(outfile); /* close output file */
}
```

REFERENCES

[Be65] Benes, V.E., *Mathematical Theory of Connecting Networks and Telephone Traffic*, Academic Press, New York, 1965.

[Co80] Conway, L. and C. Mead, *Introduction to VLSI Systems*, Addison-Wesley, 1980.

[Fr81] Franklin, M.A., "VLSI Performance Comparison of Banyan and Crossbar Communications Networks," *IEEE Transactions on Computers*, Vol. C-30, No. 4, April 1981.

[Me88] Melen, R. and J.S. Turner, "Nonblocking Networks for Fast Packet Switching," *Proceedings of the IEEE INFOCOM'89*, April 1989, pp. 548–557.

[Mo87] *MOSIS User's Manual*, University of Southern California Information Sciences Institute, Marina Del Rey, California, 1987.

[Pi75] Pippenger, N., "On Crossbar Switching Networks," *IEEE Transactions on Communications*, Vol. COM-23, June 1975.

[Ro87] Rosenberger, F. *List of Symbols for EE463 (Revision: 2.3)*, (course notes) Washington University in St. Louis, 1987.

[Va90] Valdimarsson, E. "Blocking in Multirate Networks," M.S. Thesis, Washington University, St. Louis, Missouri, May 1990.