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An Oversampled Analog To Digital Converter For Acquiring Neural Signals

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AN OVERSAMPLED ANALOG TO DIGITAL CONVERTER FOR ACQUIRING NEURAL SIGNALS

by
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ABSTRACT OF THE THESIS

A Third Order Modulator and Digital Filter for Neural Signals

by

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Master of Science in Electrical Engineering

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Research Advisor: Professor Robert E. Morley, Jr.

A third order delta-sigma modulator and associated low-pass digital filter is designed for an analog to digital converter (ADC) for sensing bioelectric phenomena. The third order noise shaping reduces the quantization noise in the baseband and the digital low-pass filter greatly attenuates the out of band quantization noise, increasing the effective number of bits. As part of a neural signal acquisition system designed by The BrainScope Company to capture Electro-Encephalogram (EEG) and Automated Brainstem Response (ABR) signals, this paper describes the design of a third order Delta-Sigma modulator which meets or exceeds the low noise specifications mandated by previous BrainScope products. The third order cascaded delta-sigma modulator attains a resolution of 12.3 bits in a signal bandwidth of 3kHz and 14.9 bits in a signal bandwidth of 100Hz, operating from a +/- 1.76V reference with a 250kHz clock.

Acknowledgments

I would like to thank the faculty at Washington University for helping me pursue my education. I would like to thank BrainScope for their financial involvement in this project. I would especially like to thank Dr. Morley for connecting me with BrainScope and for the opportunities he gave me to learn in the lab, there were plenty. I want to give a special thank you to Dr. Engel at SIU-E for his insight early in the project. I would also like to thank Ed Richter for sharing the lab with me and for his help. I would like to thank the writing center for meeting with me weekly to discuss writing strategies. Finally, I would like to extend a thank you to Washington University for helping me mature and realize my potential.

Grant Taylor Williams

Washington University in St. Louis
August 2009

Dedicated to my Mom, Dad, Laura, and Tigger.

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Chapter 1

Introduction

In processor design Moore's law states the number of transistors on a chip will double every 18 months; in quantifying performance, Intel's new standard of measurement is the performance per watt; in efficiency, it is furthering research into parallel architectures: one common fundamental trend in providing engineering solutions is making products smaller, cheaper, faster, and easier to use. In the field of bioelectric signal processing, the drive to incorporate similar qualities is very strong (Harrison and Charles 2003).

1.1 Basics of Bioelectric Signal Acquisition

Electric potentials have been known to exist in the living brain since the 1880s, but it wasn't until 1929 when a report by Berger indicated that fluctuating potentials could be detected from the scalp in a noninvasive manner (Kreezer 1938). Berger called this method of signal acquisition the electro-encephalogram (EEG). At the time, the best method of signal acquisition was to use a rudimentary type of electrode, such as a needle or silver coil sponge, then amplify the signal with tube amplifiers (Siegel 2002) and display the results with an ink-writing oscillograph (Kreezer 1938). Figure 1.1 below presents the apparatus required to record the EEG and Figure 1.2 presents a list of different types of electrodes.

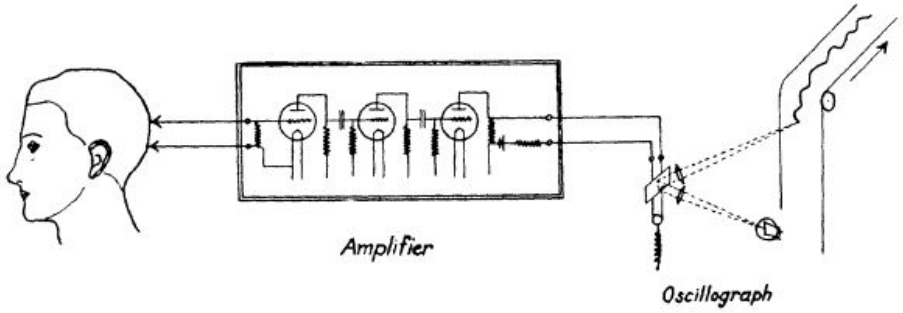

Figure 1.1 EEG Recording Apparatus, Circa 1930s (Kreezer 1938)

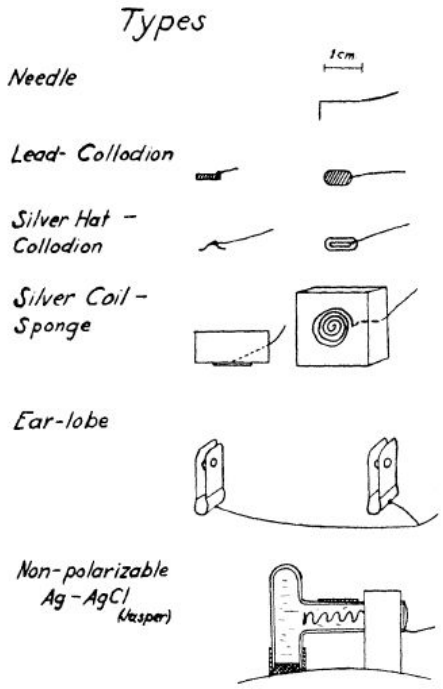

Figure 1.2 Common 1930s Electrodes for EEG Signal Acquisition (Kreezer 1938)

The chief phenomena of the EEG signals are presented in Figure 1.3 below. Alpha rhythms have a narrow bandwidth around 10Hz and beta rhythms have a narrow bandwidth around 25Hz. The alpha rhythm bandwidth is why we model the EEG as a 10Hz sine wave (Kreezer 1938).

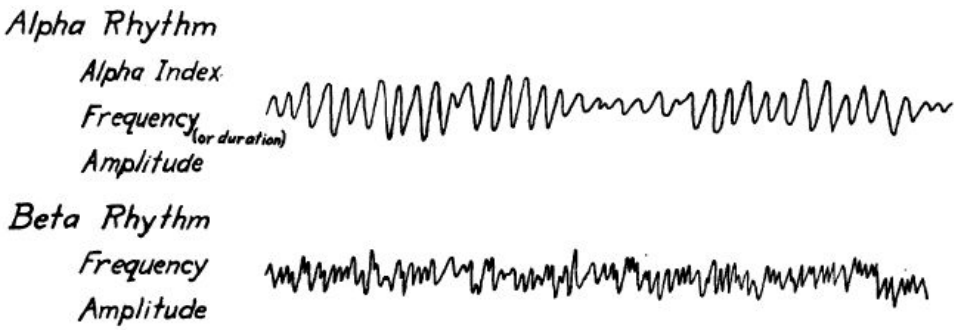

Figure 1.3 Measurable EEG Rhythms (Kreezer 1938)

Although researchers still use the silver-silver chloride electrode for signal acquisition, the later stages of signal processing that have changed drastically. The most significant change to the aforementioned acquisition chain is the ability to digitize the analog signal. Previous systems relied on analog readouts, but with current research relying so heavily on computers, analog to digital conversion is an important part of the acquisition chain. According to Harrison and Charles, there is a need among scientists and clinicians for low-noise biosignal electronics (Harrison and Charles 2003). They claim that with the advent of fully implantable multi-electrode arrays, there is an established need for fully integrated signal processing circuits (Harrison and Charles 2003). A general search of common IEEE publications such as Solid-State circuits or Transactions on Biomedical Engineering returns hundreds of low-noise neural recording Very Large Scale Integration (VLSI) designs. Figure 1.4 below presents a modern neural signal acquisition system. Step 1 is the acquisition of neural signals via the electrode. Step 2 is the chopper amplification method discussed in Chapter 2 to minimize the deleterious effects of 1/f noise, which cannot be removed entirely. Step 3 and step 4 are the analog to digital converter and digital filter/decimation stages.

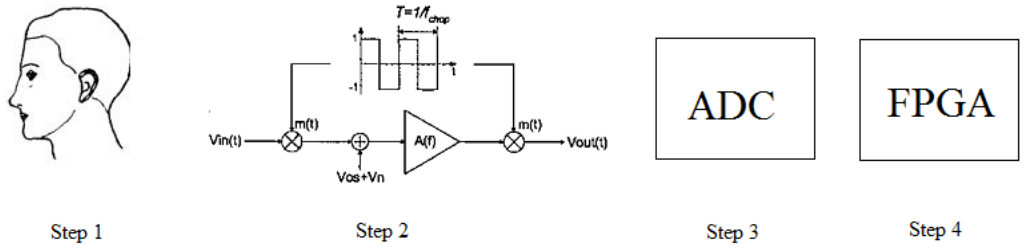

Figure 1.4 Modern Neural Signal Acquisition System

In EEG acquisition, the typical recorded signal amplitude is between 1μV and 5μV in the frequency band of interest between 0.5Hz and 100Hz (Harrison and Charles 2003; Kreezer 1938). At these low frequencies, CMOS amplifiers inherently produce flicker or (1/f) noise that swamps out the signal (Hanasusanto 2007). At high frequencies the flicker noise falls off rapidly into the white Gaussian noise floor.

In the summer of 2008, we performed a feasibility study to determine the plausibility of building an integrated circuit (IC) version of a previously designed discrete component EEG and ABR signal acquisition system (BrainScope 2008). The focus was to alleviate the problems caused by flicker noise using a chopper amplifier that modulates the low frequency signals out of the low frequency – high 1/f noise level band into a higher frequency band where signal amplification occurs. The final product of the summer feasibility study was a computer simulation of the entire process chain – from EEG signal simulation through chopper amplification, to Analog to Digital Conversion and digital filtering.

In an effort to provide BrainScope with a suitable Analog to Digital Converter (ADC) tailored specifically to the needs of EEG and ABR signal acquisition, I present a 3rd order modulator operating at 250kHz that can be placed behind a chopper amplifier in a neural signal acquisition system and deliver 12.3 bits in a signal bandwidth of 3kHz and 14.9 bits in a signal bandwidth of 100Hz.

1.2 Organization of This Thesis

This thesis is organized as follows. In Chapter 2, we discuss the theoretical calculations that determine the noise performance in a signal acquisition system and how they impact the specifications of the analog to digital converter. In Chapter 3, with the ADC performance specified, system simulation results are presented and the key tradeoff of modulator order and sampling rate is investigated. Chapter 4 presents two different hardware implementations and the corresponding measured results. In Chapter 5, an FPGA based digital filter and decimator is presented. Finally, in Chapter 6, the results of the design are summarized and the possibility of future work is presented.

Chapter 2

Theoretical Calculations

This chapter presents the background information that serves as the foundation for the bulk of the research. We first review the feasibility study of a neural signal acquisition system simulated during the summer of 2008. Some stages of the acquisition system are discussed in detail as they relate to the research either because the stage is a source of noise or because the stage establishes the noise level in the system. This chapter is significant because the analog to digital converter which we designed and is discussed in later chapters, is fully specified by the signal and noise in the preceding stages of the neural signal acquisition system.

2.1 Background

During the summer of 2008, Dr. Morley, Dr. Engel, and I were contracted by BrainScope®, Inc. to explore the feasibility of a multi-channel ASIC (Application Specific Integrated Circuit) intended to amplify, filter, and digitize both EEG and ABR signals. This section is the result of several months of work in the areas of analysis, modeling, and high-level simulation. The following paragraphs will summarize the specific results of the study which set the foundation for the oversampled ADC.

Due to Dr. Engel's extensive experience with the AMIS C5N process, CMOS technology was chosen over bipolar technology. CMOS technologies allow dense digital

circuits to be integrated on the same die as the desired analog circuitry. It is much less expensive to fabricate CMOS circuits. Moreover, high resolution analog-to-digital conversion is best achieved using CMOS. Unfortunately, relative to bipolar devices, MOS devices exhibit excessive 1/f noise characteristics (Gosselin, et al. 2004). This is unfortunate given the low-frequency signal bandwidth of the proposed design. As I will demonstrate, by using appropriate circuit techniques, any inherent limitations resulting from the choice of a CMOS technology can be effectively overcome.

The following specifications for the ASIC, in Table 2.1, were mandated by BrainScope®. Bandwidth, signal level, and Signal to Noise Ratio (SNR) are presented.

Table 2.1 ASIC Specifications from BrainScope

Signal Type	Bandwidth (Hz)	Signal Level	SNR (dB)
EEG	0.5 Hz – 50 Hz	10 μVp-p	20 dB
ABR	100 Hz – 3 kHz	1 μVp-p	0 dB

2.2 Signal Modeling

Two models for the EEG signal were used throughout this work. The simple signal is a 10 Hz sine wave, with peak amplitude of 5 μV, representing the minimal signal level. A more realistic signal is generated by passing white noise through a 7th-order ARMA (Auto-Regressive Moving Average) filter (Janeczko and Lopes 2000). The output waveform is then low-pass filtered and used to simulate alpha rhythms. A typical EEG waveform (time-domain) is illustrated in Figure 2.1. The associated frequency-domain spectrum is presented in Figure 2.2. Note the dominant spectral peak at approximately 10 Hz. This peak is the motivation for the simple model.

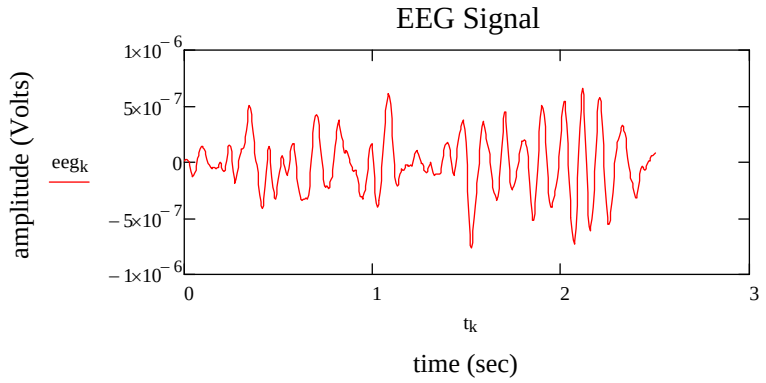

Figure 2.1 Representative alpha rhythm EEG signal used in simulation

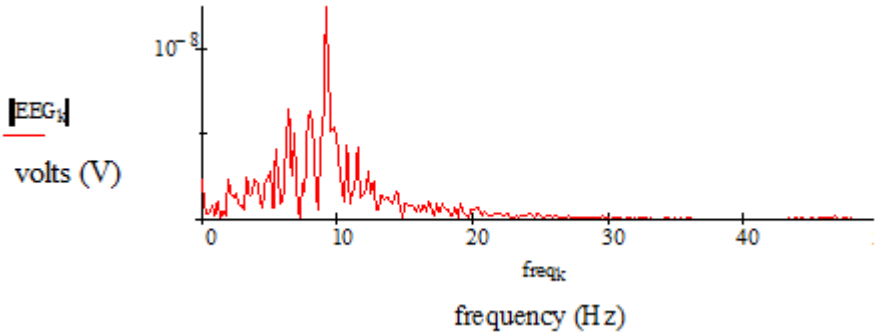

Figure 2.2 Spectrum of EEG signal presented in Figure 2.1

The realistic ABR signal was modeled using Bessel functions (Nunez 1973) as illustrated in Figure 2.3, below.

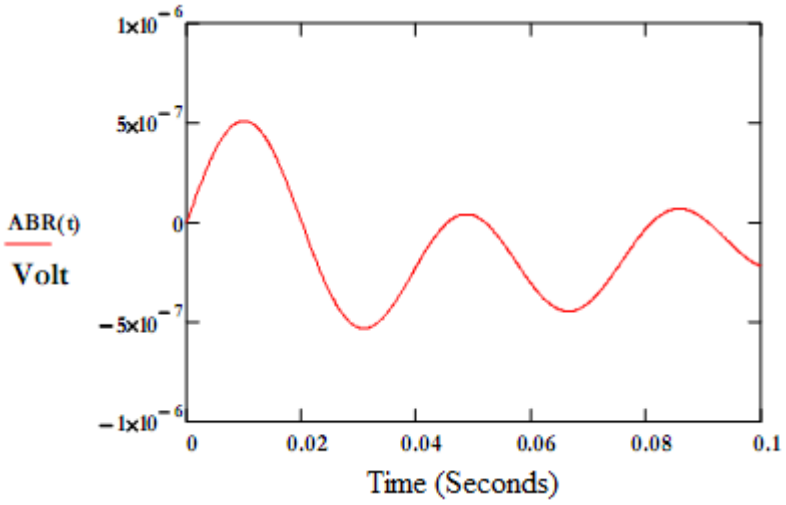

Figure 2.3 Realistic ABR signal used in simulations

2.3 Chopper Amplifier

As explained earlier, the very poor 1/f noise characteristics of the FETs in a CMOS process influence the design of the pre-amplifier to limit the noise delivered to the ADC. The technique most effective in suppressing low-frequency noise for this application is chopper stabilization (CHS) (Temes and Enz 1996). The chopper stabilization technique applies modulation to translate the signal to a higher frequency where there is less 1/f amplifier noise and then demodulate it back to baseband after amplification. For simplicity, the modulation is performed using a square-wave carrier. After chopping/modulating, the signal is translated to odd harmonic frequencies of the chopping/modulating signal. After amplification, the signal is demodulated using the same square-wave carrier that was used for the initial modulation. While the input signal is modulated, amplified, and then demodulated, the input-referred CMOS amplifier noise and offset voltages are modulated only once, limiting the total noise at the output of the amplifier and the input of the ADC. Figure 2.4 below presents a 15Hz sine wave after a chopping by a 16kHz square wave. The signal is transposed from 15Hz to 16kHz +/- 15Hz where the 1/f noise is much smaller.

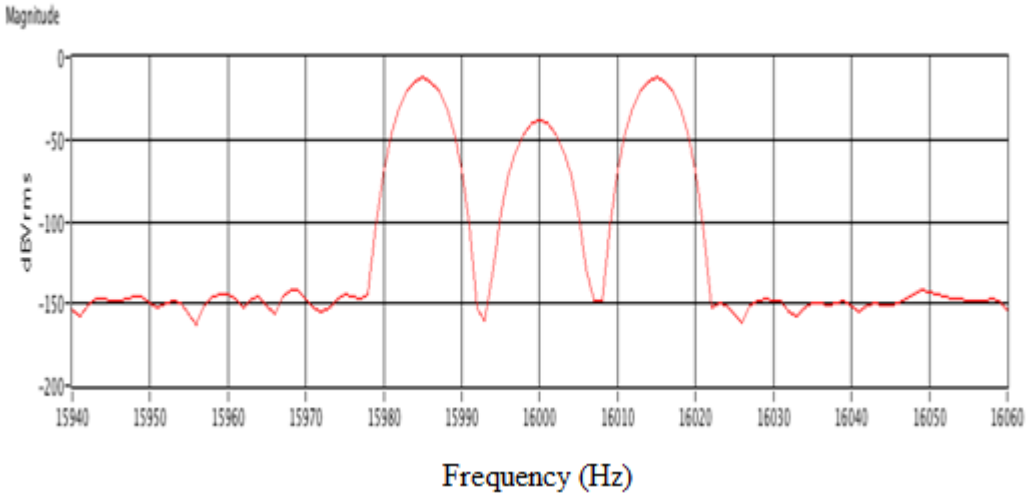

Figure 2.4 A 15Hz Sinusoid, Chopped by a 16kHz Square Wave

The purpose of this thesis is to develop a continuous time modulator with low pass digital filter that meets or exceeds the specifications of the current BrainScope design. In Figure 2.5, the input-referred noise characteristics (red solid line) of the Linear Technologies' LTC1127 instrumentation amplifier used in current BrainScope® designs are compared with those of a pre-amplifier that one is able to design using the AMIS C5N process (blue dotted line) without the use of chopper stabilization.

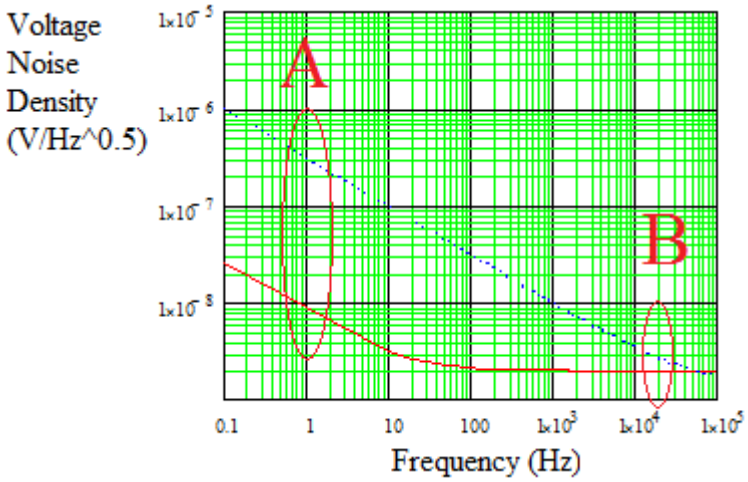

Figure 2.5 1/f noise comparison of current BrainScope design and AMIS C5N CMOS process without chopping

The 1/f noise of a preamplifier in the C5N process is very large, outlined as the difference between blue and red in the 'A' region. One can easily see that the integrated noise (area under the curve) for the C5N preamplifier is much larger than that of the LTC1127. What chopper stabilization effectively does is allow one to replace the total integrated 1/f noise in the baseband (0.5 Hz – 100 Hz) with the total integrated 1/f noise in a narrow band near the chopper frequency of 16kHz. The 1/f noise in region 'B' is much less than in region 'A'.

The noise performance (total integrated noise, input-referred) in EEG mode (bandwidth of 0.5 Hz to 100 Hz) is summarized in Table 2.2 while the noise performance in ABR (bandwidth of 100 Hz to 3kHz) is summarized in Table 2.3 (Engel 2008).

Table 2.2 Summary of Noise Performance for EEG signals

	LTC	Our design without CHS	Our design with CHS
1/f	184 nV	7.3 μV	0.251 μV
Thermal	200 nV	0.149 μV	0.149 μV
Total	272 nV	7.3 μV	0.291 μV

Table 2.3 Summary of Noise Performance for ABR signals

	LTC	Our design without CHS	Our design with CHS
1/f	148 nV	7.3 μV	1.4 μV
Thermal	1.1 μV	0.814 μV	0.814 μV
Total	1.1 μV	7.3 μV	1.7 μV

The goal is to ensure at least a 20 dB signal-to-noise ratio for the lowest amplitude EEG signals (5μV) at the output of the amplifier and input to the ADC. Using the simple model for the EEG signal (a 10 Hz sine wave), this amplitude corresponds to an RMS level of 3.5 μV. Given the above noise characteristics (291μV) and the 20dB SNR specification, 3.5μV results in 22dB of SNR. For ABR signals, where the RMS value is as small as 350 nV, the "one-shot" SNR is actually negative (-14 dB). The negative SNR is acceptable, since ABR signal recognition is accomplished through the averaging of hundreds to thousands of frames, improving the SNR to near 0 dB (Engel 2008). Averaging improves the SNR because ABR is a repetitive signal buried in uncorrelated noise. Averaging the uncorrelated noise reduces it relative to the correlated ABR signal.

The predicted noise performance of the proposed design is based on some assumptions but going into them is not within the scope of this thesis (Engel 2008). Appendix A

presents the detailed account of the assumptions. The results above in Tables 2.2 and 2.3 represent worst-case values and somewhat better performance is possible.

2.4 Delta-Sigma Modulator

The most appropriate type of ADC for use in applications requiring low output sample rates but very high resolution are delta-sigma over-sampling converters. This style of converter trades off accuracy in time for accuracy in amplitude and makes use of noise shaping (Allen and Holberg 2003). The guiding design equation for delta-sigma converters is

$$DR = \sqrt{\frac{3OSR^{2L+1}}{2pi^{2L}}(2L+1)} \qquad (2.1)$$

where DR is the achievable dynamic range of the ADC, OSR is the oversampling ratio, and L is the order of the modulator. Once the achievable dynamic range is computed, then the effective number of bits (ENOB) for resolution purposes may be calculated using

$$ENOB = \frac{\log\left(\frac{DR}{\sqrt{3}}\right)}{\log(2)} + 0.5 \qquad (2.2)$$

We investigated and simulated modulators of different order and decided the 3rd order modulator operating at a sampling frequency of 256 kHz would satisfy the requirements mandated by BrainScope. Little additional area is required to implement a 3rd order modulator and the sampling frequency required is not as high as when a 2nd order modulator is used. The third integrator is generally much smaller than the integrators needed to realize the 2nd order modulator (Engel 2008).

For ABR signals where the bandwidth of interest is 3 kHz, the Nyquist sampling rate is 6 kHz. If the modulator operates at 256 kHz, the OSR is 43. For a 3rd order modulator, from (2.1) the resulting DR is 95 decibels and from (2.2) the ENOB is 15.4 bits. For EEG signals (where the bandwidth of interest is 100 Hz) the ENOB is 32.5 bits; however, the performance in reality will be determined by the analog characteristics (noise, finite gain, finite bandwidth) of amplifiers used in the modulator. Even for EEG signals, the achievable ENOB is likely to be on the order of 15 or 16 bits (Engel 2008).

For EEG signals, it is predicted that the total integrated input-referred noise is roughly 300 nV. After applying an effective gain of 175 the noise level at the input to the modulator is 50 μV. For ABR signals, the predicted total integrated input-referred noise is 1.7 μV. After the effective gain of 175, the noise level at the input to the modulator is 300 μV. Table 2.4 below summarizes the noise level present at the input to the ADC.

Table 2.4 Predicted Noise Level at the Input of Analog to Digital Converter

Fs (kHz)	Noise BW (Hz)	Total Integrated Noise (VRMS)	ENOB (Bits)
256 kHz	3 kHz	300 μV	11.23
256 kHz	100 Hz	50 μV	13.8

One way of implementing higher-order modulators is to cascade multiple lower-order stages in such a way that each stage processes the quantization noise of the previous stage (Allen and Holberg 2003). In cascade modulators, outputs of the individual stages go to digital error cancellation circuitry where the quantization noise of previous stages is attenuated and the quantization noise of the remaining stage is high pass filtered. We selected a second-order stage followed by a first-order stage because it is less sensitive to circuit imperfections than most other cascade structures (Wooley and Rabii 1997).

Chapter 3

System Simulation

This chapter presents the background information that serves as the foundation for the bulk of the research. We first review the feasibility study of a neural signal acquisition system simulated during the summer of 2008. Some stages of the acquisition system are discussed in detail as they relate to the research either because the stage is a source of noise or because the stage establishes the noise level in the system. This chapter is significant because the analog to digital converter which we designed and is discussed in later chapters, is fully specified by the signal and noise in the preceding stages of the neural signal acquisition system.

3.1 Mathematical Analysis of Proposed Architecture

Once the analysis had determined the use of an oversampled ADC, we decided to begin with a design by Rabii and Wooley that maintained large full-scale input range while avoiding signal clipping at internal nodes. The Rabii and Wooley publication also presented a method for CMOS implementation which would be useful for future extensions of this research project (Wooley and Rabii 1997). Figure 3.1 below shows the signal flow diagram of the system.

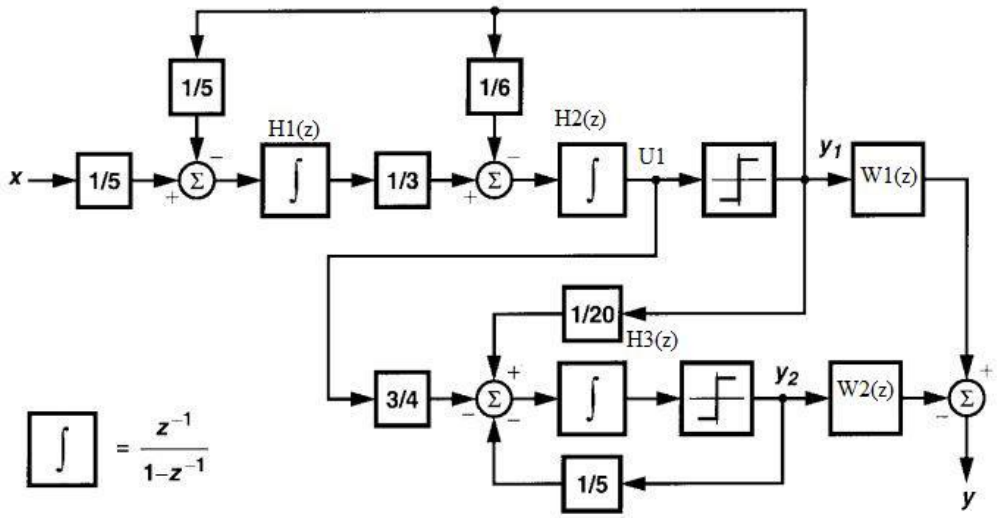

Figure 3.1 Rabii and Wooley Sigma Delta Modulator Architecture (Wooley and Rabii 1997)

We performed an analysis of the 1997 Rabii and Wooley architecture and determined that in order to solve for the third order transfer function, a transformation to a similar architecture presented in a 1994 paper by Williams and Wooley was necessary. Below, Figure 3.2 shows the 2-1 architecture from the 1994 publication.

Notice how the signal flow diagram from 1994 is nearly identical to the 1997 diagram. According to Williams and Wooley, an equivalent transformation is featured in Figure 3.3 below.

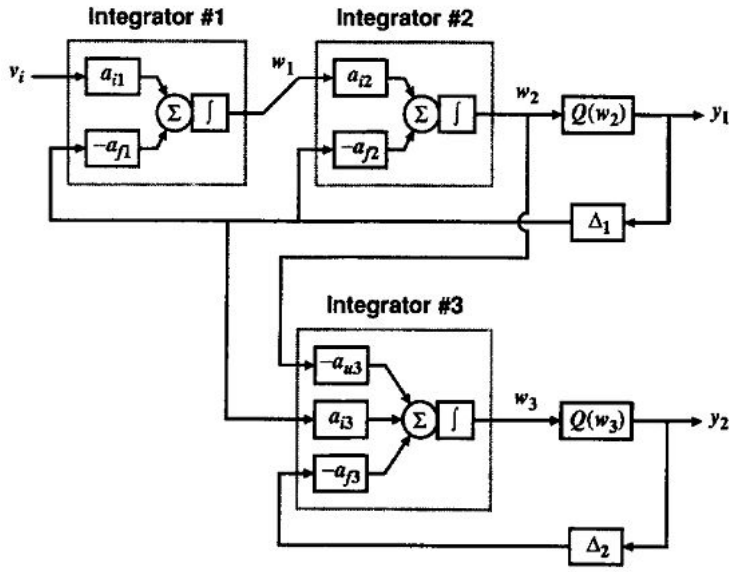

Figure 3.2 Williams and Wooley, 1994 2-1 Architecture Implementation [Woo:94]

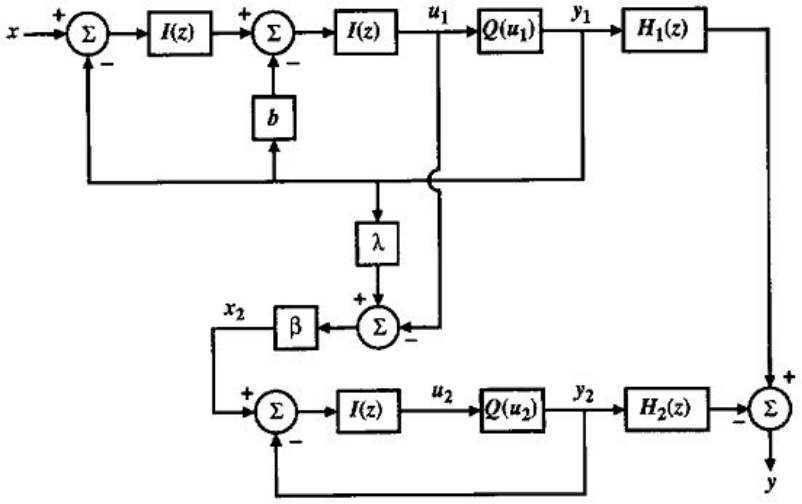

Figure 3.3 Williams and Wooley, 1994 2-1 Architecture [Woo:94]

Using the following equations, featured in Equation 3.1 below, the appropriate transformation can be made to arrive at the transfer function in Equation 3.2.

$$\boldsymbol{x} = \frac{\boldsymbol{a_{i1}}}{(\boldsymbol{a_{f1}\Delta_1})}\boldsymbol{v_i}$$

$$\boldsymbol{b} = \frac{\boldsymbol{a_{f2}}}{(\boldsymbol{a_{f1}a_{i2}})} \qquad (3.1)$$

$$\boldsymbol{\beta} = \frac{\boldsymbol{a_{f1}\,a_{i2}a_{u3}}}{\boldsymbol{a_{f3}}}\left(\frac{\Delta_1}{\Delta_2}\right)$$

$$\boldsymbol{\lambda} = \frac{\boldsymbol{a_{i3}}}{(\boldsymbol{a_{f1}a_{i2}a_{u3}})}$$

$$\boldsymbol{Y(z) = X(z) + \ (1 - z^{-1})^3 * \left[\frac{\left(a+1-b+\frac{1}{G_2}\right)E_1(z)}{G_1} - \frac{\frac{1}{\beta}E_2(z)}{G_2}\right]} \qquad (3.2)$$

The transfer function features the most important characteristic of the 2-1 architecture: the ability to cancel out the first stage error term by appropriately selecting 'a' and combining the error cancelation filters H1 and H2 presented in Equation 3.3 below.

$$H_1(z) = z^{-1}(1 - a(1 - z^{-1}))$$
$$H_2(z) = \frac{1}{\beta}(1 - z^{-1})^2 \qquad (3.3)$$

According to the 1997 Rabii and Wooley publication, the H1 transfer function is simply a delay, suggesting that 'a' = 0. G1 and G2 are 0.5973 and 1.08, respectively, and beta is 0.25.

3.2 Matlab Analysis of Transfer Function

The transfer function derived in the previous section is plotted in Figure 3.4 below. The blue trace is filtered 2nd order response, the green trace is the filtered 1st order response, and the red trace is the resulting third order response, generated by the subtraction of the 1st order from the 2nd order.

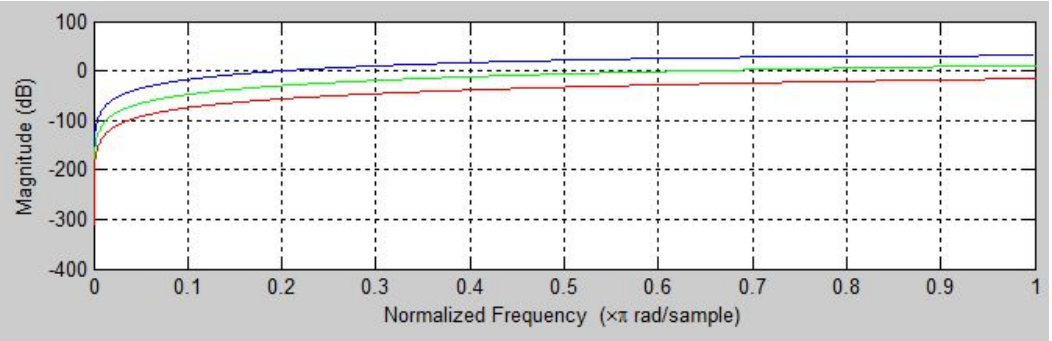

Figure 3.4 Matlab Transfer Function of 1997 Rabii and Wooley ADC – Blue is filtered 2nd order, green is filtered 1st order, red is resulting 3rd order

3.3 LabVIEW Simulation

With the mathematical foundation in place, the simulation focus shifted to LabVIEW. Figure 3.5 below shows the virtual instrument (VI) that implements the third order modulator of Figure 3.1 above. This VI is referred to as an ideal VI because it does not

account for analog noise and instead presents the results of shaping quantization noise only. Later, this VI will be modified to accept analog noise for more accurate simulations.

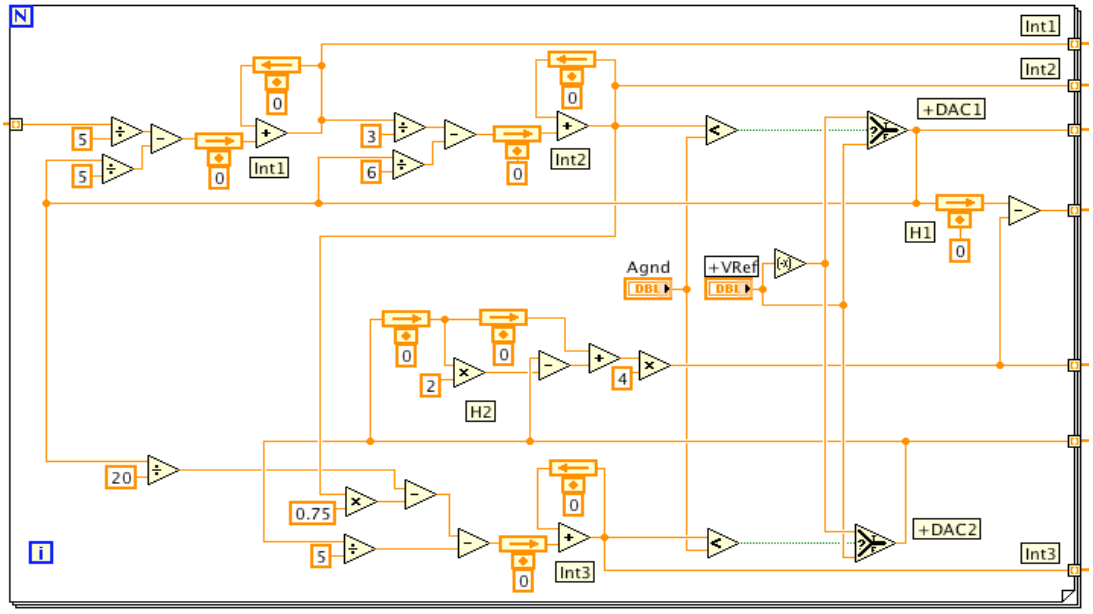

Figure 3.5 Rabii and Wooley Virtual Instrument programmed in LabVIEW

In order to evaluate the results of the system, a test VI, shown in Figure 3.6 below, was created which passes in the simple EEG signal as an input, varies the phase of the sinusoid (such that the finite state machine does not put out the same results each time) and displays the results.

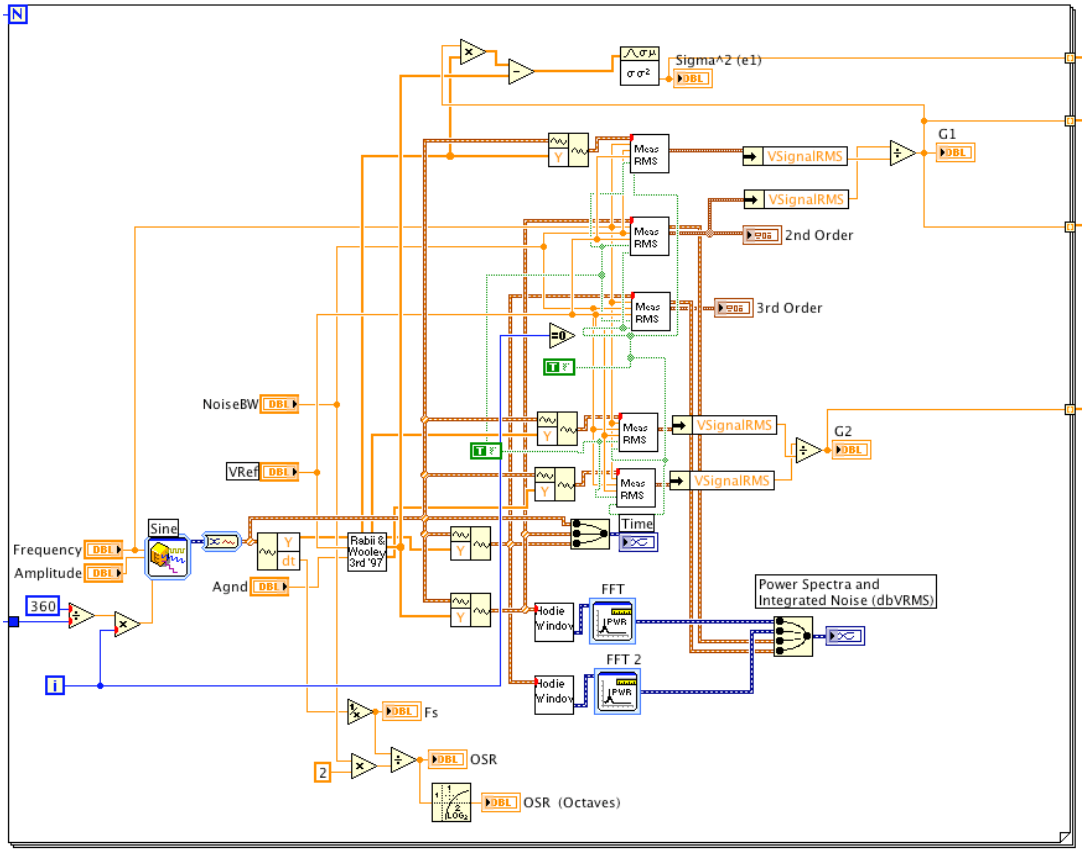

Figure 3.6, Rabii and Wooley Test Virtual Instrument

The virtual instrument provides a general idea of the shaping of quantization noise, shown in Figures 3.7 and 3.8 below with the power spectrum and integrated noise of the 2nd and 3rd order outputs. The frequency axis is set to the maximum bandwidth of interest, 3kHz. The important feature to notice is that the 3rd order performance is superior to the 2nd order performance, as in Figure 3.4.

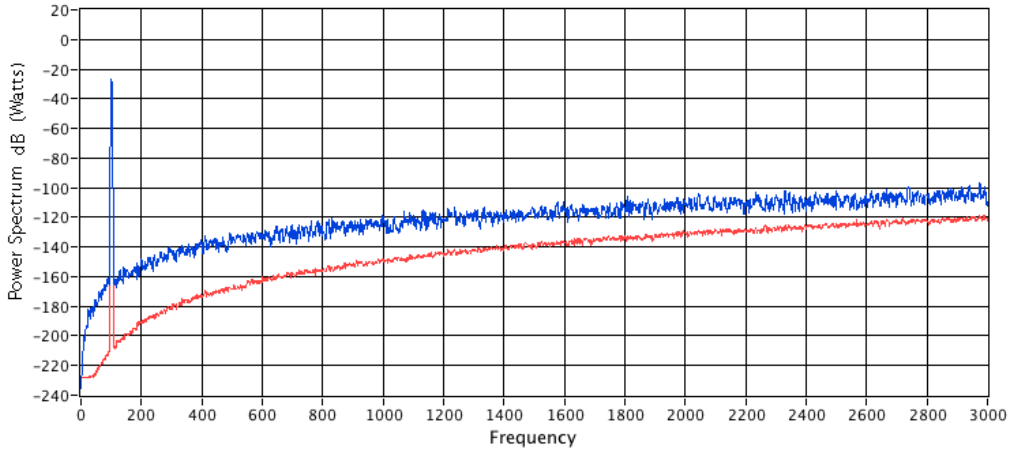

Figure 3.7 LabVIEW's Ideal Wooley ADC, Power Spectrum, Signal (100Hz Tone) and Shaped Noise 2nd Order Output in Blue, 3rd Order Output in Red

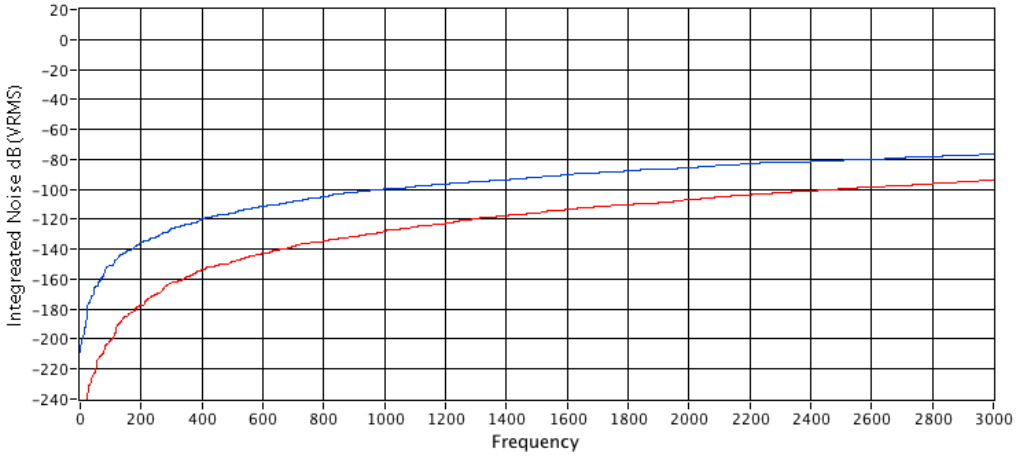

Figure 3.8 LabVIEW Ideal Wooley ADC, Integrated Noise, 2nd Order Blue, 3rd Order Red

Table 3.1 below summarizes the results for the ideal (quantization noise only) 2nd and 3rd order designs.

Table 3.1 Rabii and Wooley Ideal LabVIEW Results (Quantization Noise Only)

Order	VNoiseRMS	NumBitsFS	NoiseBW	OSR
3rd	20.08u	13.8	3kHz	42.6
2nd	145.2u	10.9	3kHz	42.6

3.4 Multisim Simulation

Having demonstrated acceptable performance with the discrete time LabVIEW simulations, we turned to circuit level simulation of the modulator. NI Multisim is an electronic schematic capture and simulation program which implements the traditional SPICE circuit simulation software designed at Berkeley (Multisim 2009).

The Multisim schematic for the 3rd order modulator is presented in Figure 3.9 below. For Multisim simulations the input is a sine wave passed into a cascaded 2nd order and 1st order integrator op-amp represented by part U4, a comparator represented by parts U1 and U2, and a digital flip-flop to sample and hold the output, represented by parts U5 and U7.

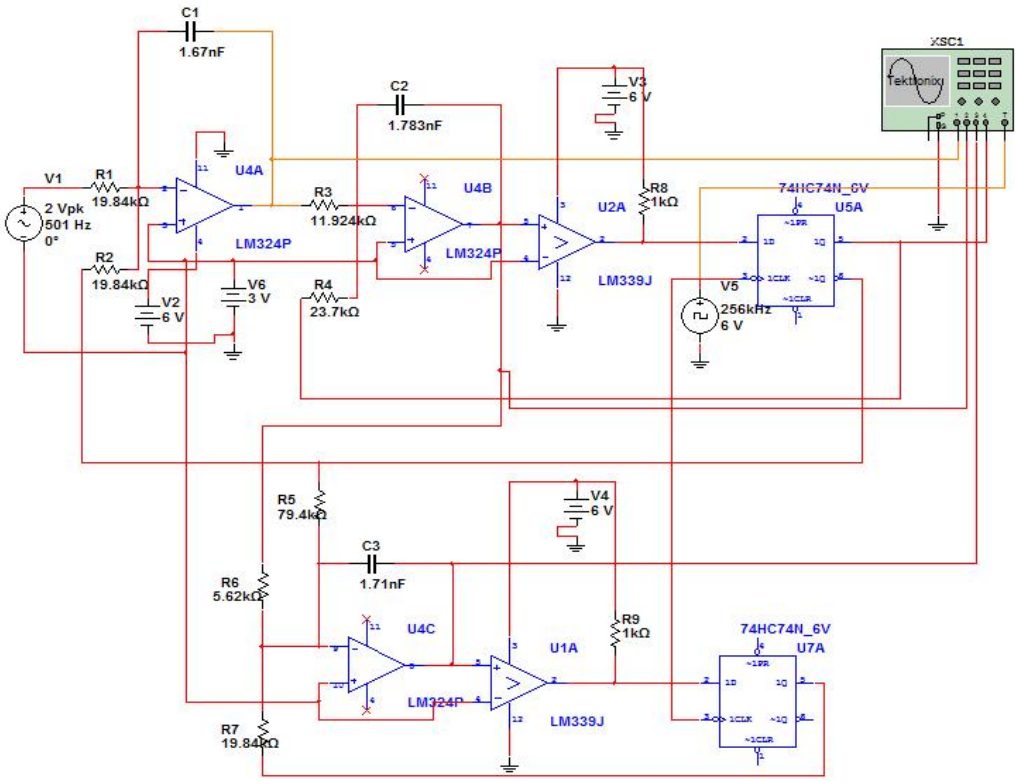

Figure 3.9 Multisim Circuit Schematic for Wooley Delta-Sigma Modulator

Saving the output from terminal 1Q of both flip-flops, we used the LabVIEW environment to implement the digital error cancellation filter to generate the 3rd order signal. The exact same virtual instrument used to implement the digital filter for the ideal Rabii and Wooley architecture was used with the Multisim signals.

Figures 3.10 and 3.11, below, show the power spectrum and integrated noise for 2nd and 3rd order Multisim associated with the Multisim simulation. The results are presented in Table 3.2, following the figures.

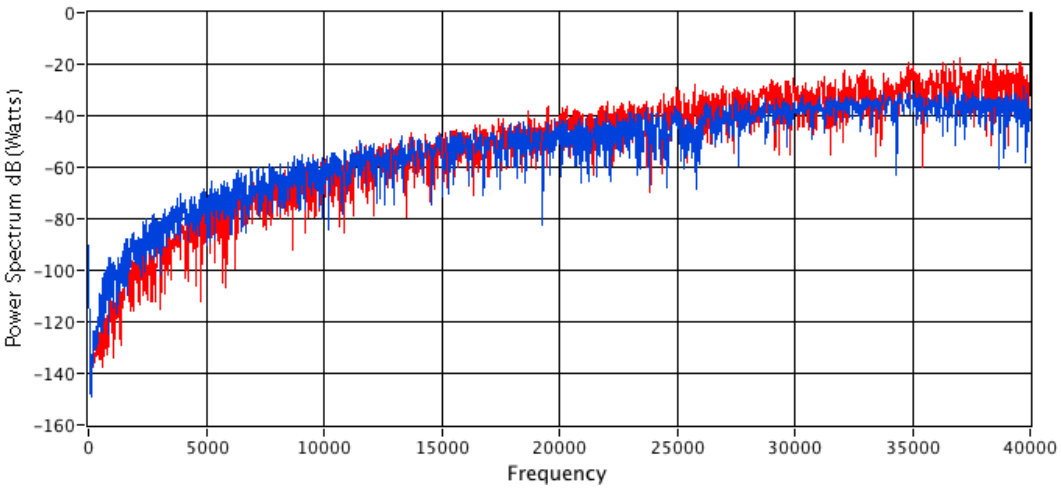

Figure 3.10 Power Spectrum for Multisim Circuit Schematic Modeled After 1997 Rabii and Wooley, 2nd Order in Blue, 3rd Order in Red

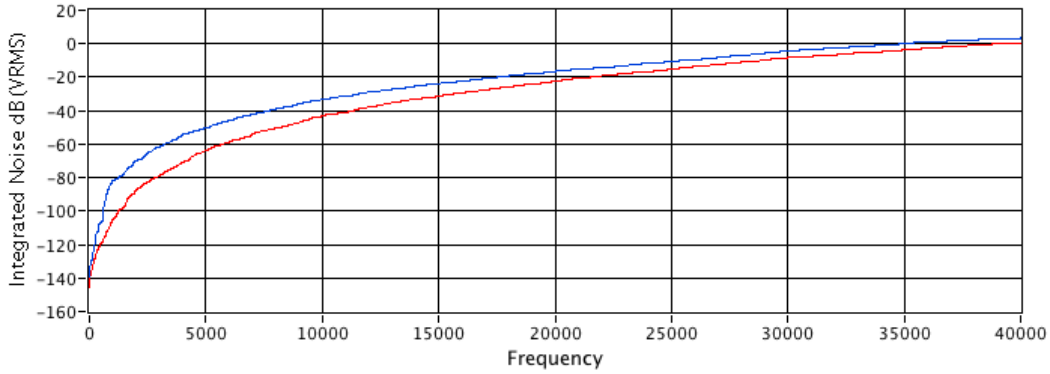

Figure 3.11 Integrated Noise for Multisim Circuit Schematic Modeled After 1997 Rabii and Wooley, 2nd Order in Blue, 3rd Order in Red

Table 3.2 Multisim 3rd Order Noise Shaping Simulated Results

Order	VNoiseRMS	NumBitsFS	NoiseBW	OSR
3rd	111 μV	13.9	3kHz	42.6
3rd	0.170 μV	23.3	100Hz	1250

3.5 System Simulation Summary and Results

Presented below in Table 3.3 are the BrainScope requirements and the results of the simulations, indicating that the 2-1 architecture simulated by LabVIEW and Multisim is in fact acceptable in terms of ENOB. Differences in integrated noise are due to different reference voltages. The ENOB is always calculated as full scale ENOB.

Table 3.3 The Performance Requirements Mandated by BrainScope and Results (F_s = 256kHz)

Fs 256kHz	Source	Noise BW (Hz)	Total Integrated Noise (VRMS)	ENOB
	BrainScope Specification	3 kHz	300 μV	11.23
	BrainScope Specification	100 Hz	50 μV	13.8
	LabVIEW Sim	3kHz	20.08 μV	13.8
	Multisim Simulation	3kHz	111 μV	13.9
	Multisim Simulation	100Hz	0.170 μV	23.3

Chapter 4

Circuit Design, Fabrication, and Testing

The previous chapter indicated that the circuit simulation of Rabii and Wooley 2-1 architecture compared well with the mandated BrainScope performance. We then developed a hardware based implementation. This chapter presents how we built a printed circuit board and measured the performance.

4.1 Bread Board 2nd Order Modulator

Figure 4.1, below, presents the first breadboard implementation we built. Despite being on a solderless experiment board featuring an onboard clock, mid-rail generator, and strategies that are easily implemented and offer somewhat lower performance than PCB implementation. The design is a good starting block for early comparisons to the Multisim simulations. Later in this chapter, we will detail how an improved implementation reduced the noise.

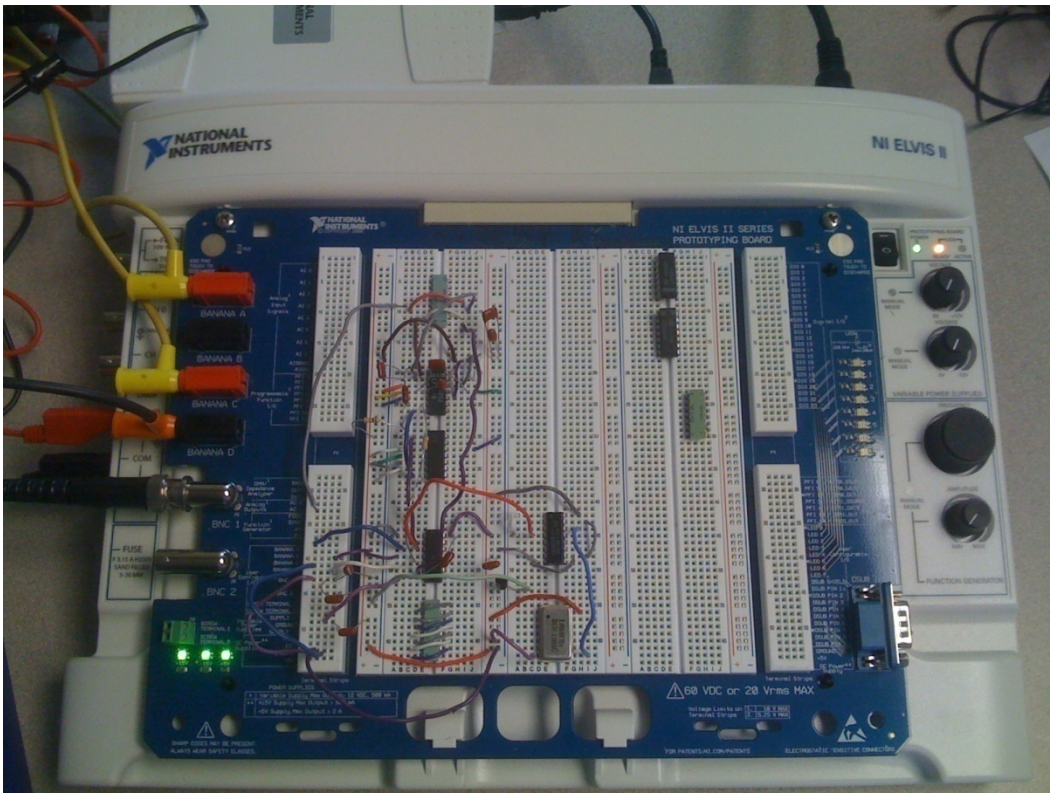

Figure Figure 4.1 Solderless Bread Board Implementation of the Multisim Schematic in Figure 3.9

Due to the nature of the setup, using the NI Elvis as a breadboard interface prevented the capture of both flip flop outputs because there was only one available channel with which the computer could capture data. The following results are presented for the 2nd order performance only. However, since this was the first time we could measure the analog noise, later we will present a method which predicts the 3rd order bread board performance using the analog noise as a parameter. Below, Figures 4.2 and 4.3 present the measured integrated noise and power spectrum for the breadboard modulator operating at 250kHz. Table 4.1, after the figures, presents the results.

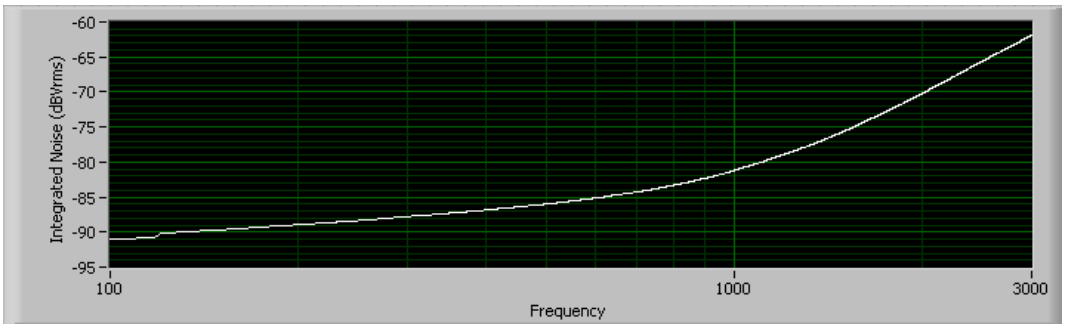

Figure 4.2 Measured Integrated Noise from Breadboard Modulator Operating at 250kHz

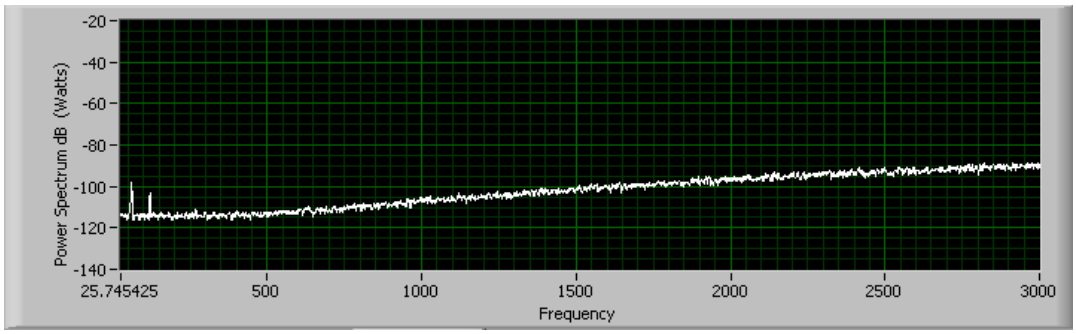

Figure 4.3 Measured Power Spectrum (with 60Hz and Harmonics) from Breadboard Modulator Operating at 250kHz

Table 4.1 Measured Results from Breadboard Modulator Operating at 250kHz

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB
2	250 kHz	3 kHz	800 μV	10.8 Bits
2	250 kHz	100 Hz	30 μV	15.6 Bits

Compared to 10.9 bits performance that the ideal LabVIEW VI simulation predicted, the 2nd order measured performance of 10.8 bits is close. The following measurement is from the same modulator operating at 500kHz. Figures 4.4 and 4.5 below present the integrated noise and power spectrum, followed by Table 4.2 with results.

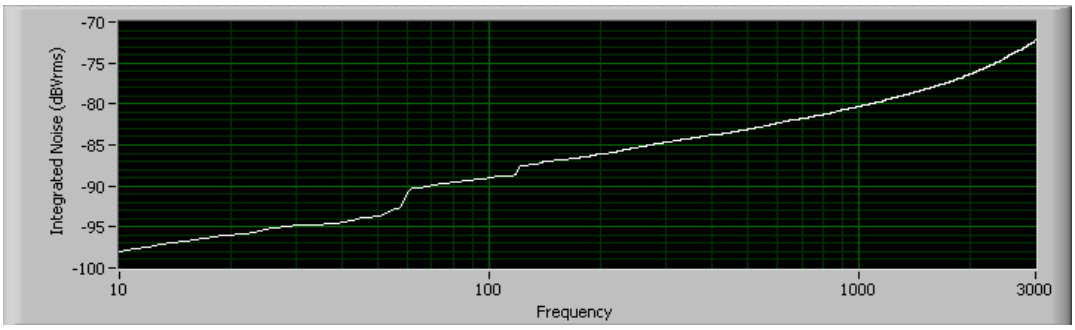

Figure 4.4 Measured Integrated Noise from Breadboard Modulator Operating at 500kHz

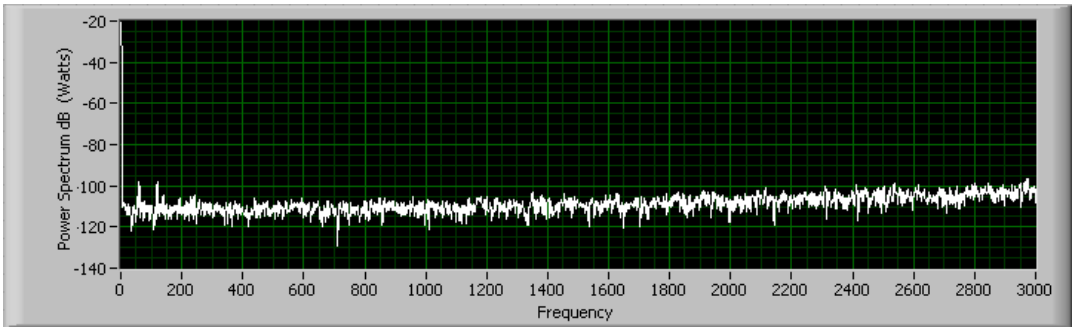

Figure 4.5 Measured Power Spectrum (with 60Hz and Harmonics) from Breadboard Modulator Operating at 500kHz

Table 4.2 Measured Results from Breadboard Modulator Operating at 500kHz

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB
2	500 kHz	3 kHz	300 μV	12.6 Bits
2	500 kHz	100 Hz	35 μV	* 15.3 Bits

* The reason the ENOB did not change when the OSR doubled is because of the flat noise floor in that bandwidth of interest. The purpose of oversampling at 500kHz was

to confirm this result which implies the dynamic range is White Noise Limited – there is no shaping.

As expected, the effective number of bits increased with a doubling of the oversampling ratio. According to BrainScope, only 11.23 bit performance is required for a noise bandwidth of 3kHz, so for now, a possible solution is to take the 2nd order output when the modulator operates at 500kHz. However, the system is not fully characterized. The 3rd order output must be compared to the 2nd order output in order to determine the proper hardware based implementation.

4.2 Bread Board 3nd Order Modulator

Since the 3rd order performance could not even be measured with the breadboard configuration and NI Elvis, the above second order performance measurements were obtained without any concern to 3rd order performance, meaning the 3rd order op-amp terminals were grounded on the first breadboard. We implemented strategies to simulate the performance of the 3rd order portion to help determine whether the modulator should operate at 250kHz or 500kHz. By measuring the analog noise associated with the 2nd order measurements, we were able to modify the ideal Wooley LabVIEW virtual instrument simulation, which originally had no analog noise and only measured quantization noise, to accept an input referred analog noise parameter and predict the performance of 3rd order noise shaping. The logic is that if I can input a level of noise that causes the simulated 2nd order output to perform identically to the measured 2nd order performance, then the simulated 3rd order performance would theoretically match the measured 3rd order performance.

As a reminder and reference of performance, the 2nd order breadboard results are presented again below in Table 4.3. Note that these measured results as they will be compared and shown to be the same as the results from the modified LabVIEW simulation which includes analog input noise.

Table 4.3 Measured Performance of 2nd Order Breadboard Rabii and Wooley ADC

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB
2	250 kHz	3 kHz	800 μV	10.8 Bits
2	500 kHz	3 kHz	300 μV	12.6 Bits
2	250 kHz	100 Hz	30 μV	15.6 Bits
2	500 kHz	100 Hz	35 μV	15.3 Bits

Table 4.4 below presents the results from the LabVIEW simulation with analog input noise included. As a reminder, the 2nd order performance has been established by the breadboard results and should be confirmed in the simulation below. The 2nd order results compare well with the breadboard results, indicating that with the same analog noise, the simulated 3rd order performance results are likely to be accurate predictors of measured results.

Table 4.4 A Comparison of the 2nd and 3rd Order Performance from LabVIEW Simulation

Order	Fs (kHz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB (Bits)	Optimum Choice
2	250 kHz	3 kHz	800 μV	10.9	
3	250 kHz	3 kHz	800 μV	13.1	*
2	250 kHz	100 Hz	30 μV	15.6	
3	250 kHz	100 Hz	30 μV	15.6	*
2	500 kHz	3 kHz	240 μV	12.5	
3	500 kHz	3 kHz	240 μV	12.8	
2	500 kHz	100 Hz	35 μV	15.4	
3	500 kHz	100 Hz	35 μV	15.4	

The results from the breadboard measurements indicate what is necessary to meet the specifications. At 250 kHz, the 2nd order breadboard results indicate extra bits for EEG but not enough bits for ABR, so we decided that the ADC should have 3rd order noise shaping. With 3rd order shaping, there is no considerable improvement in ENOB when sampling at 500 kHz due to a white noise limitation, so we decided that the sampling frequency should be 250 kHz.

4.3 Bread Board Optimization Strategies

The breadboard design we implemented was similar to the Multisim circuit seen earlier in this thesis. However, we improved the hardware based solution in the following ways. First, we replaced the slow (1.3MHz Gain Bandwidth Product), noisy (40nV/Hz1/2) LM324with a faster (4MHz Gain Bandwidth Product), less noisy (15nV/Hz1/2) JFET input LF347 op-amp. Second, we replaced the slow LM339 comparator with a high speed TLC3702 comparator. Finally, the digital flip flops were removed and implemented in an FPGA with a 'return to zero' scheme that delivers uniform charge packets to the integrator to improve linearity.

Figure 4.6 below shows the circuit schematic, modified to reflect the changes above. The output of the two comparators feed into an FPGA for digital processing, and the output of the FPGA feeds back into the circuit via Q1X/Q1Y/!Q2X/!Q2Y – signals used to implement the return to zero procedure. Also below is Figure 4.7, an oscilloscope screen capture of a sequence of uniform charge packets, confirming the return to zero method.

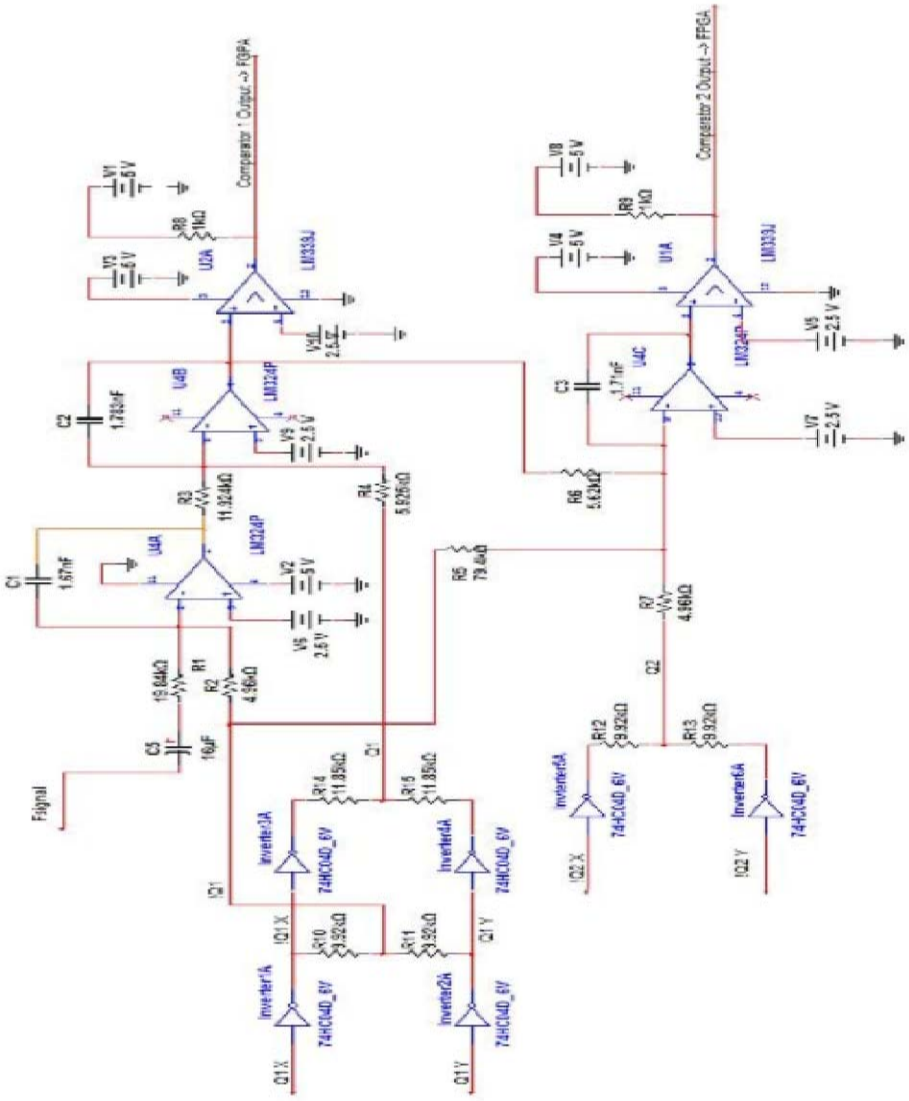

Figure 4.6 Modified Circuit Schematic, Showing the Return to Zero Architecture

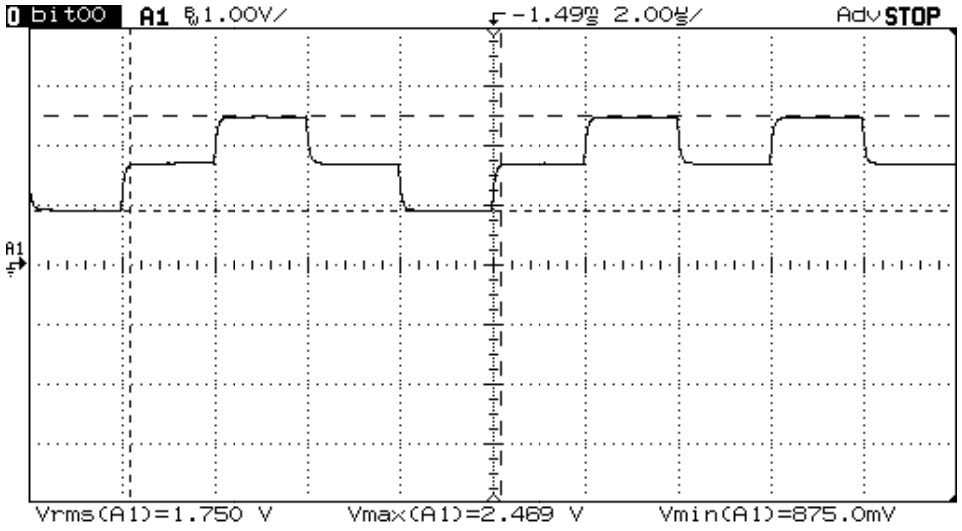

Figure 4.7 A Sequence of Uniform Charge Packets

Figure 4.8 below presents the final configuration for measuring the performance of the breadboard Rabii and Wooley modulator. On the right is the breadboard configuration corresponding to the circuit diagram in Figure 4.6, above, in the middle is a Spartan-3E FPGA evaluation board, and on the left is a breakout board connected to a National Instruments High Speed Digital I/O card in the computer. After the modifications were implemented, the performance of the modulator was confirmed to show the Verilog on the FPGA worked.

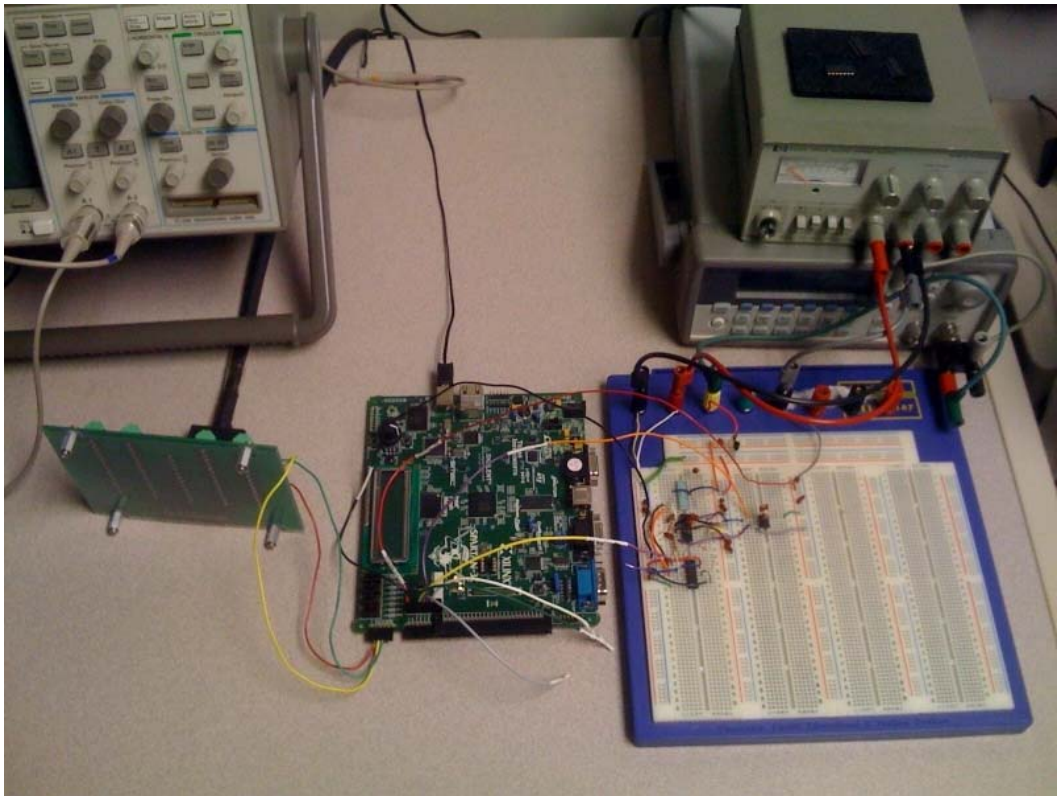

Figure Figure 4.8 Rabii and Wooley ADC Configuration Featuring: Breadboard, FPGA, National Instruments High Speed Digital I/O Card from Right to Left

4.4 Printed Circuit Board Implementation

Having achieved suitable results with the breadboard design, the next step was to move to a design that would interface easily with the FPGA and be more compact with lower noise. We employed freely available software called PCB Express (PCB 2009) to design a printed circuit board 71mm by 41mm. One advantage of the printed circuit board over the breadboard is that the design can easily be replicated and extra boards can be printed provided by emailing the Gerber file to a factory. More importantly, we expect superior performance due to short PCB traces reducing noise.

Figures 4.9 and 4.10 below present the schematic and corresponding layout created using the PCB Express software. There are two male hex single inline connectors placed to align with two female hex single inline connectors on the FPGA board used to provide communication and power between the PCB and FPGA. Also, a BNC connector was placed on the modulator PCB to allow connection of the input to the modulator. In the layout figure, two layers of the four layer board are designated ground and power supply voltage planes.

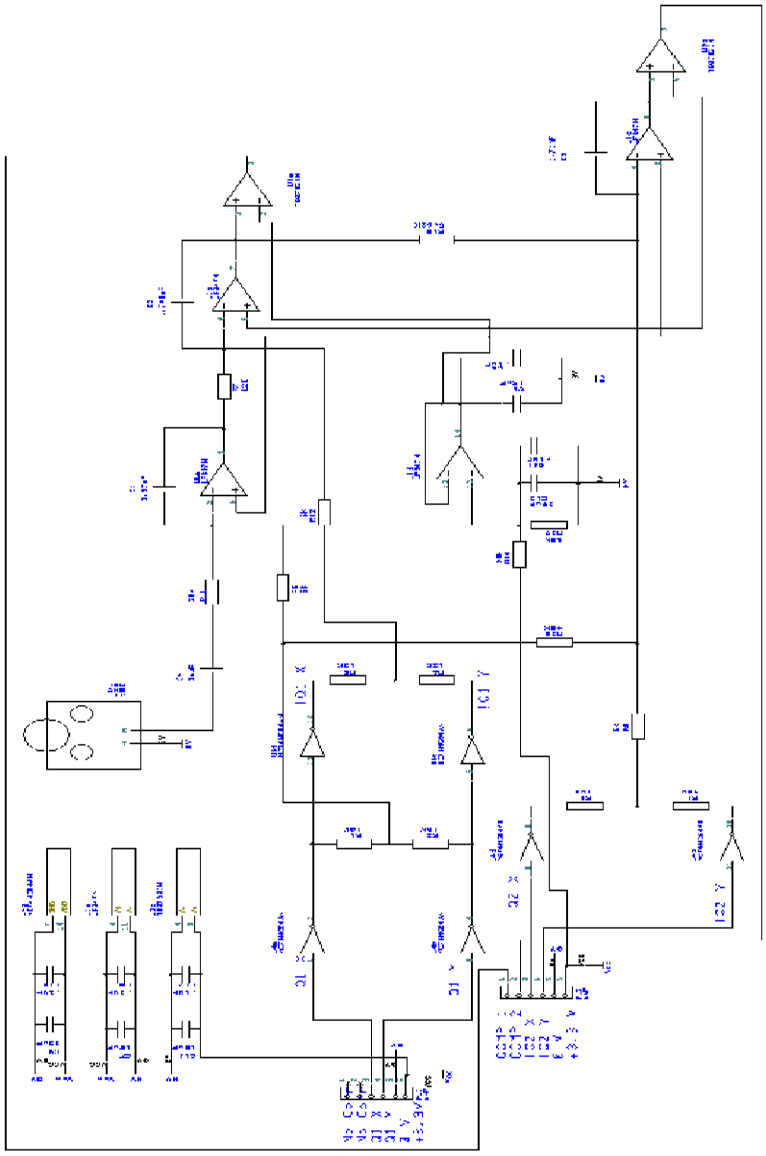

Figure 4.9 Printed Circuit Board Schematic of Rabii and Wooley Continuous Time ADC

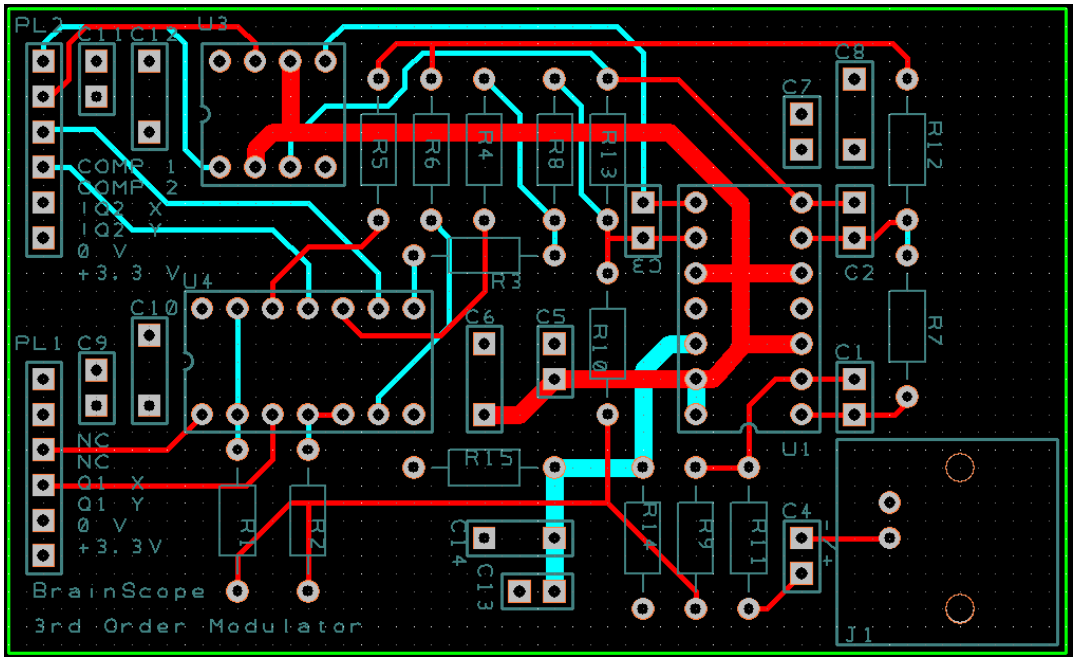

Figure 4.10 Printed Circuit Board Layout, Corresponding to the Schematic Above

Figure 4.11 below presents the final system configuration including the FPGA board on left and the modulator PCB on right, together eliminating the need for a breadboard and stand alone power supply. You can see that for the configuration shown below, the PCB is designed to connect to the two SIP hex connectors on the FPGA board.

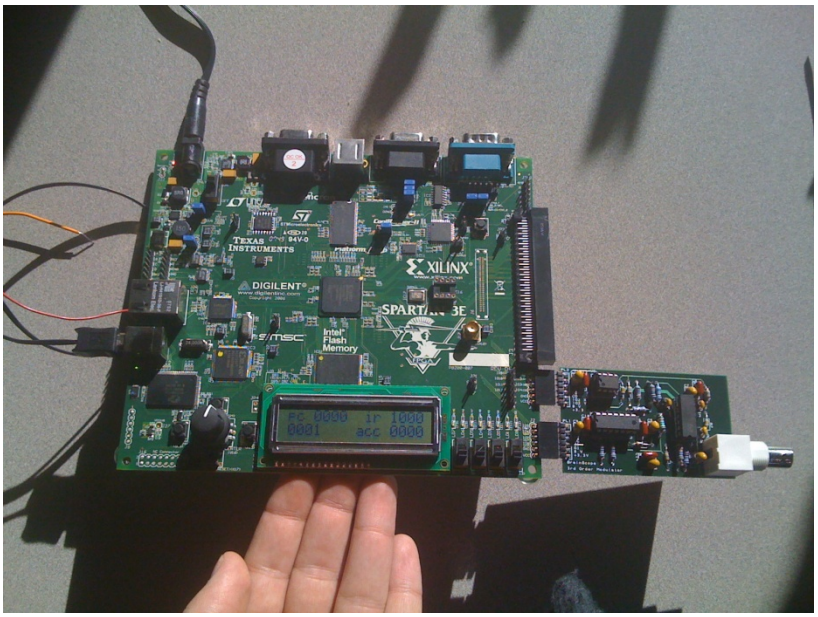

Figure 4.11 PCB and FPGA Wooley Modulator

Figures 4.12 and 4.13 below present the integrated noise and power spectrum for the printed circuit board for the 2nd order Rabii and Wooley modulator. Table 4.5 presents the measured noise results which indicate that the printed circuit board measures the same amount of noise as the breadboard in 3kHz of bandwidth. The breadboard measured 300μV and the printed circuit board measured 309μV.

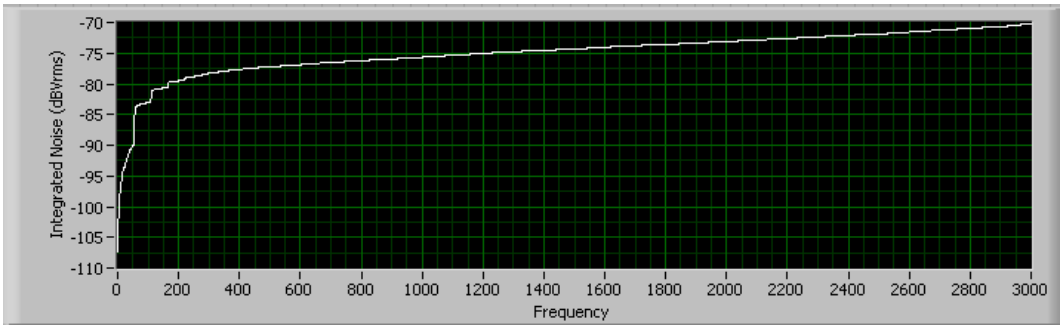

Figure 4.12 Measured Integrated Noise for 2nd order PCB Rabii and Wooley Operating at 500kHz

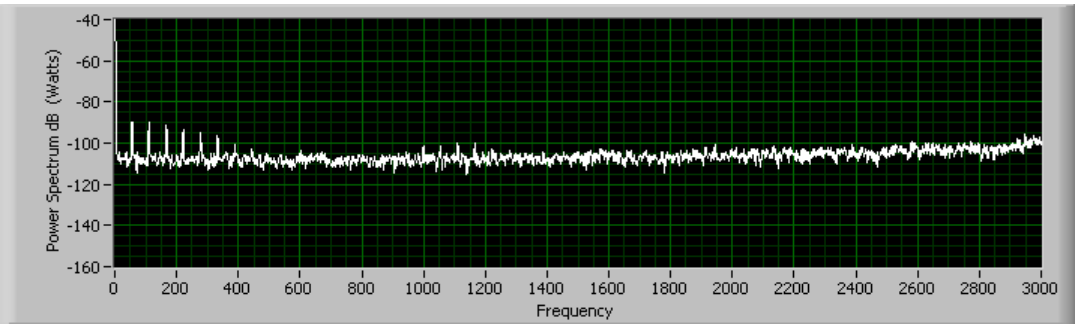

Figure 4.13 Measured Power Spectrum (with 60Hz and harmonics) for 2nd order PCB Rabii and Wooley Operating at 500kHz

Table 4.5 Measured Results for 2nd Order PCB Rabii and Wooley Operating at 500kHz

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB (Bits)
2	500 kHz	3 kHz	309 μV	11.7 Bits

Below, Figures 4.14 and 4.15 show the integrated noise and power spectrum for a 2nd order and error cancelled 3rd order. In this case, the error cancellation was performed as a virtual instrument in LabVIEW. For these figures, the modulator operated at 250kHz. Table 4.6 listing the results follows. The 3rd order performance is on the mark, better than BrainScope's noise requirement.

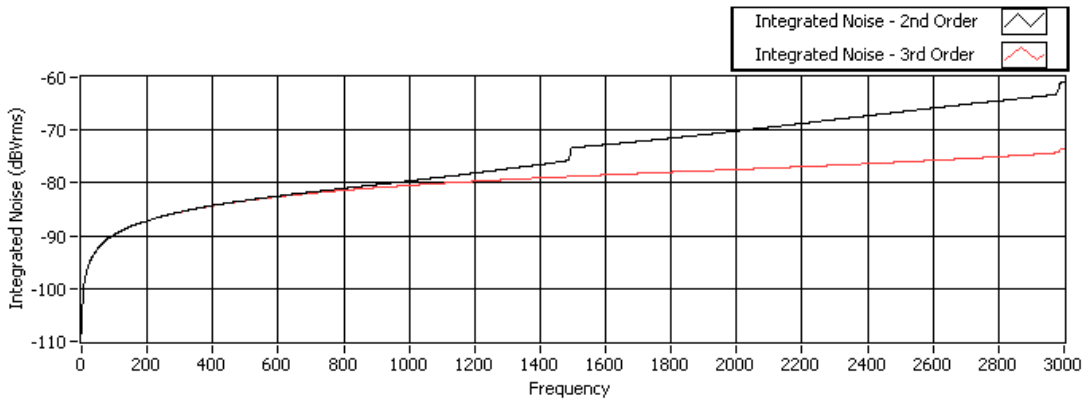

Figure 4.14 Measured Integrated Noise for PCB Rabii and Wooley ADC

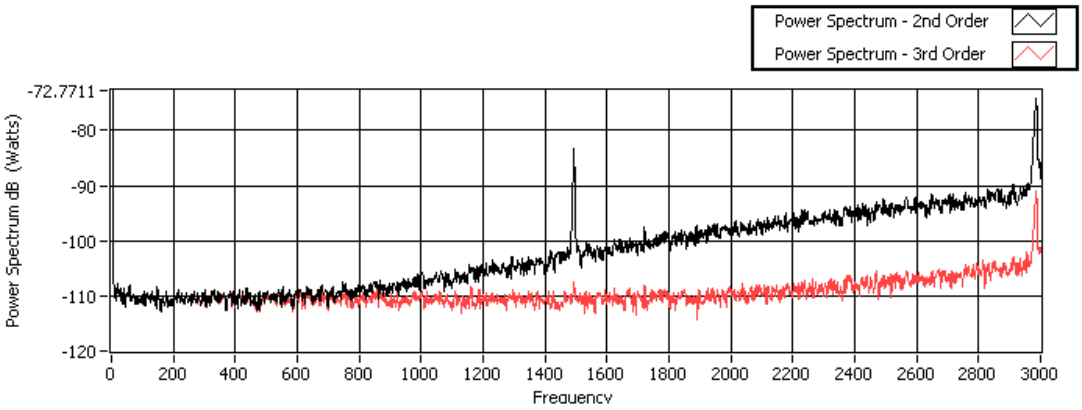

Figure 4.15 Measured Power Spectrum (with spurious tones) for PCB Rabii and Wooley ADC

Table 4.6 Measured Results for PCB Rabii and Wooley ADC

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB (Bits)
2	250 kHz	3 kHz	897 μV	10.1 Bits
3	250 kHz	3 kHz	210 μV	12.2 Bits
2	250 kHz	100 Hz	33 μV	14.9 Bits
3	250 kHz	100 Hz	33 μV	14.9 Bits

Chapter 5

Digital Filter

In Chapter 4, a hardware based solution was presented demonstrating that both breadboard and printed circuit board designs of Rabii and Wooley's modulator performed as well as one another and compared well with the simulated LabVIEW ADC. In this chapter, we perform error cancellation in the FPGA. Also, decimation and low pass filters are designed and discussed including how to integrate them in the FPGA. Finally, results are presented, discussed, and compared to simulations.

5.1 Sample Something

In previous sections, the error cancellation procedure was implemented in LabVIEW as a virtual instrument. Below, Equation 5.1 presents how the 2nd order and 1st order outputs are combined to create the proper 3rd order output. The correctly combined output is H1(z) – H2(z).

$$H_1(z) = z^{-1} \qquad (5.1)$$
$$H_2(z) = 4(1 - z^{-1})^2$$

Figures 5.1 and 5.2 below present the integrated noise and power spectrum for the PCB Rabii and Wooley ADC with error cancellation on the FPGA. Table 5.1 lists the results.

In the 3kHz bandwidth of interest, the noise level is the same as in the previous section when H1 and H2 were combined in LabVIEW. However, in the 100Hz bandwidth, the performance is not the same, with about a 60μV difference between the two cases. Upon closer inspection, the increase in integrated noise around the 60Hz region is much larger (15dB) in this measurement compared to previous measurements (6dB). A difference of 9dB is 1.5 bits which would make the measured 13.5 bits equal to 15 bits, spot on with previous measurements of 14.9 bits.

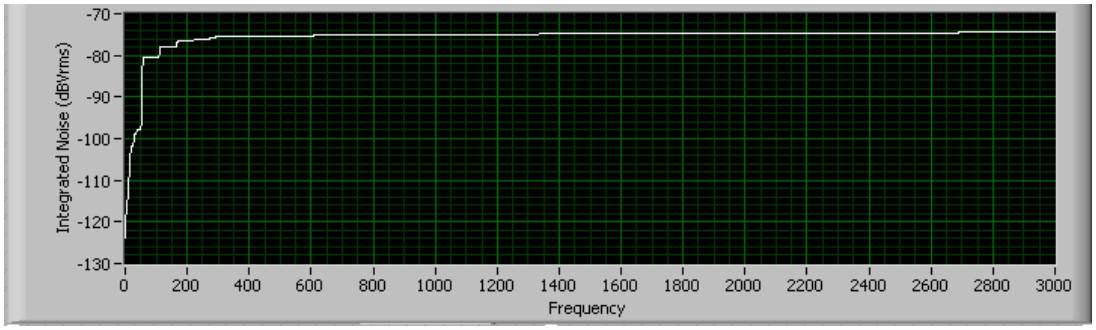

Figure 5.1 Measured Integrated Noise for PCB Rabii and Wooley ADC with Error Cancellation on FPGA

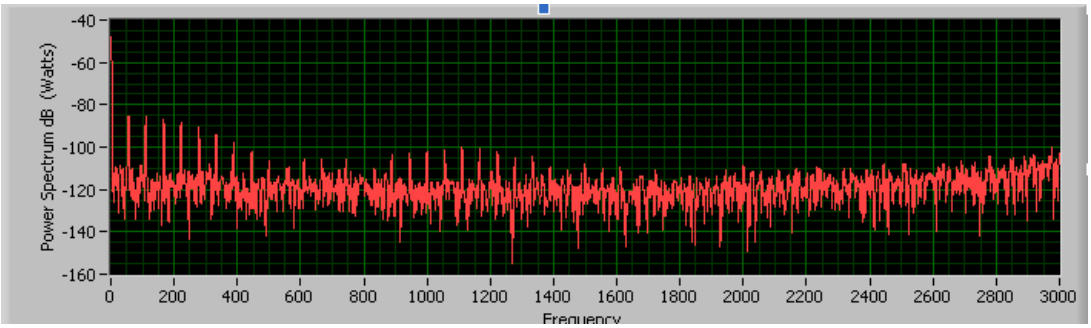

Figure 5.2 Measured Power Spectrum for PCB Rabii and Wooley ADC with Error Cancellation on FPGA

Table 5.1 Measured Results for PCB Rabii and Wooley ADC with Error Cancellation on FPGA

Order	Fs (Hz)	Noise BW (Hz)	Total Integrated Noise (Volts)	ENOB (Bits)
3	250 kHz	3 kHz	195 μV	12.3 Bits
3	250 kHz	100 Hz	90 μV	13.5 Bits

Due to the constraint of only a few available pins on the FGPA, the error cancelled third order output was sent serially to the LabVIEW environment. To facilitate the parallel to serial interface in Verilog, a clock operating at 2.5MHz places each shifted bit of the output value onto the pin to be captured by LabVIEW. The timing diagram for this operation is presented in Figure 5.3 below. The serialized data consists of Q1, Q2, six bits of combined and error cancelled third order output, and two zero values. Six bits are enough to represent the finite number of outputs.

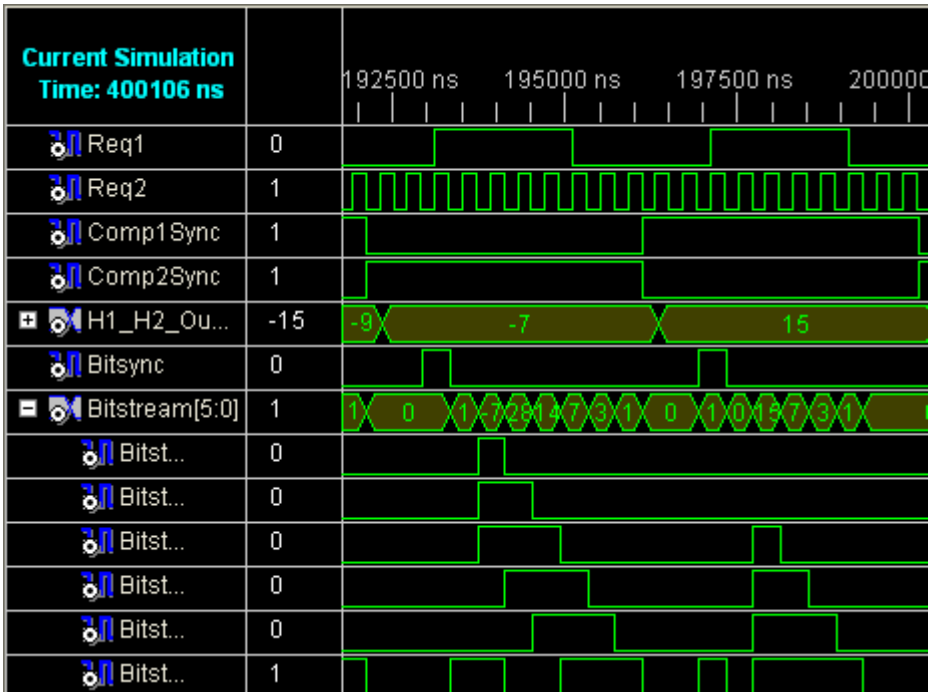

Figure 5.3 Timing Diagram Showing A Sync Pulse and the Serialized Bit stream

5.2 Decimation Filter

The decimation and low pass digital filter stage is an important part of the oversampled ADC chain. The purpose of this stage is to remove the shaped quantization noise which is above the signal bandwidth. The simplest filter for reducing input sampling rate at the first stage is the Sinc filter, which corresponds to a moving average or rectangular window low pass FIR filter having the length of decimation factor (Tenhuhen et al. 1990). According to Wooley and Vleugels, for a modulator of order L, a cascade of K=L+1 Sinc filters will provide nearly complete attenuation of the aliased quantization noise at 4 times the Nyquist rate (Wooley and Vleugels 2002). Following the Sinc filter is a standard low pass Finite Impulse Response (FIR) filter, sometimes half-band in nature with even coefficients set to zero making the filter easier to implement digitally. Half-band filters have a decimation factor of two. There are two distinct filter stages, one for ABR and one for EEG. Presented below are the two proposed methods. Figure

5.4 below shows the proposed method for ABR and EEG. The Nyquist rate for ABR and EEG are 6kHz and 200Hz, respectively.

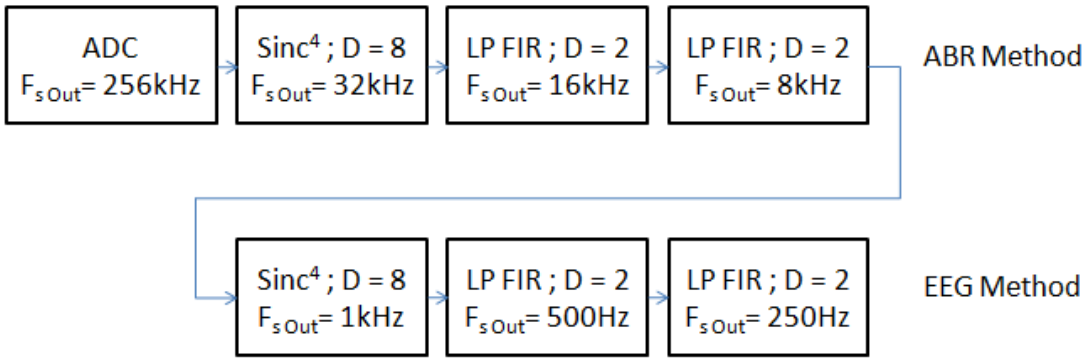

Figure 5.4 The proposed method of filtering and decimation to the Nyquist rates

With the aforementioned information in hand, a sample filter chain is described and simulated in LabVIEW with the results presented below. Figures 5.5 through 5.8 present different stages of the filtering and decimation process. Figure 5.5 presents the power spectrum for an unfiltered signal and a Sinc4 filtered signal. Figure 5.6 presents the power spectrum for the decimated signal of Figure 5.5. Figure 5.7 presents the power spectrum for the FIR filtered signal and Figure 5.8 presents the decimated version.

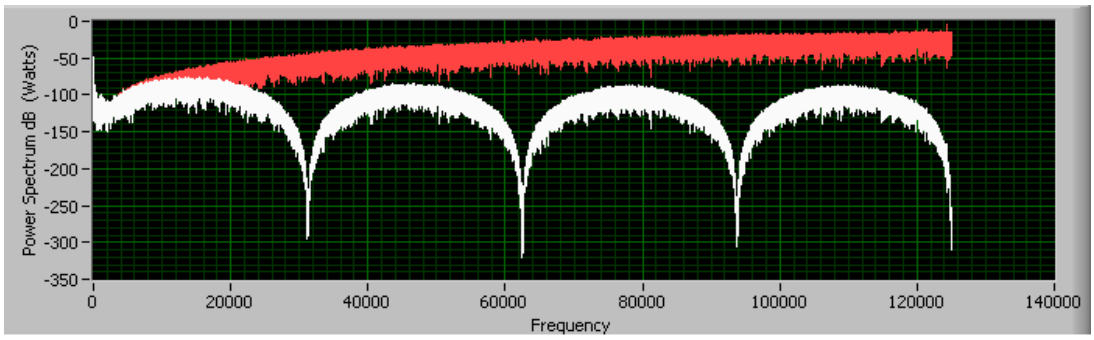

Figure 5.5 Unfiltered Power Spectrum in Red and Sinc^4 Filtered Power Spectrum in White

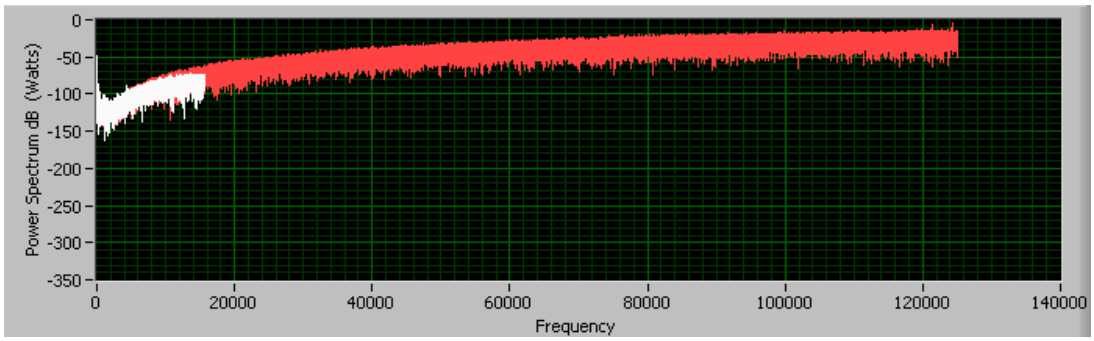

Figure 5.6 Unfiltered Power Spectrum in Red and Sinc^4 Filtered and Decimated Power Spectrum in White

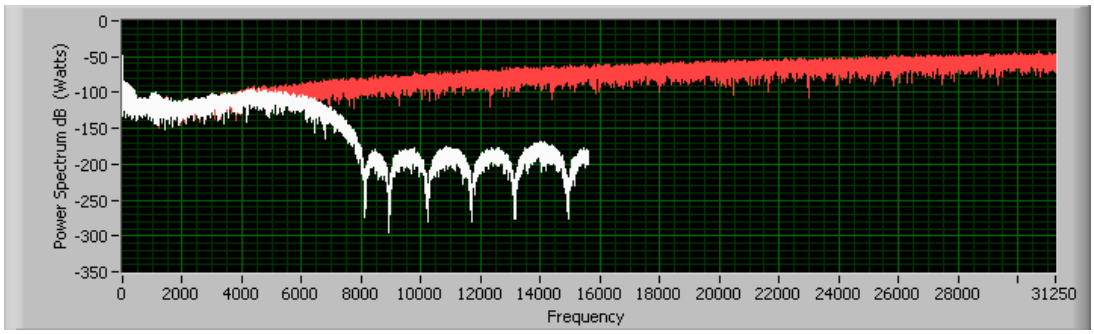

Figure 5.7 Unfiltered Power Spectrum in Red and Sinc4 Filtered, Decimated, and FIR Filtered Power Spectrum in White

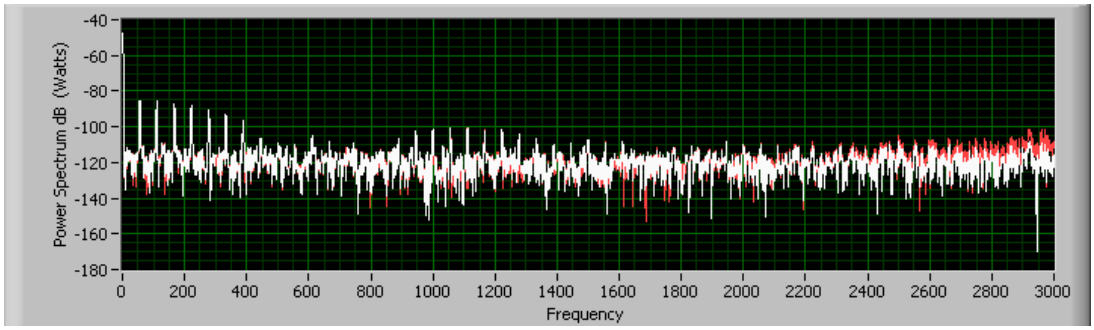

Figure 5.8 Unfiltered Power Spectrum in Red and Sinc4 Filtered, Decimated, FIR Filtered, Decimated, Power Spectrum in White

Chapter 6

Conclusions

Based on the measured experimental results from the printed circuit board, it was presented that the neural signal ADC satisfies the requirements set forth by BrainScope to deliver 11.2 bits with about 300 μV of noise in 3kHz and 13.8 bits with about 50 μV in 100Hz. The PCB described in Chapter 4 delivers 12.2 bits and 210 μV of noise in 3kHz and 14.9 bits and 33 μV of noise in 100Hz.

6.1 Areas for Future Investigation

In Chapter 5, we showed that the Sinc4 filter followed by FIR filters attenuated the out of band quantization noise and prevented aliasing. Future work can be done to implement these architectures in the FPGA. There is also an opportunity to employ the use of an available 32 pin header interface on the FPGA that would alleviate the problems caused by having too few digital input/output pins. It is evident that the future work will continue to employ strategies to minimize noise and miniaturize the printed circuit board presented in this paper. The Rabii and Wooley design can be scaled down to sub micron CMOS technology and the Verilog can be retargeted from the FPGA to a standard cell ASIC library.

It was mentioned at one point that BrainScope has to acquire 8 channels of neural data, which would require an expansion of the design in the following areas. First, the PCB based modulator was designed to capture a single channel and would need to be replicated 7 times to be able to acquire 8 signals. This procedure can easily be done using the PCB Express software. A 32 pin header matching the FPGA header would be created to interface with the FPGA board instead of the two hex connectors. In Verilog, the design would have to change as well, replacing the parallel to serial code with code that accounts for 8 incoming signals. Strategies should be investigated about how to minimize FPGA resource usage (gate count) while expanding to 8 channels of DSP. One strategy is to use half-band FIR filters which would halve the number of digital multiplies. Tradeoffs should be compared to determine if one FGPA or many FPGAs would be required.

Appendix A

MOS Noise Performance

The performance assumes a two-stage core amplifier design (with a bandwidth twice that of the chopper i.e. 32 kHz) in which the size of the compensation capacitor determines both the power consumption and the thermal noise performance of the amplifier. Increasing the size of the compensation capacitor improves thermal noise performance. Use of a larger compensation capacitor; however, increases both the power used and area occupied by the core amplifier. In Table 2.2, a value of 10 pF was assumed for the compensation capacitor (two are needed because the core amplifier is fully differential). Use of a larger value (30 or 40 pF) would help improve overall performance in both modes to some extent. The 1/f noise performance was estimated under the assumption that no single FET should occupy an area more than about 300 μM^2. Once again use of larger devices could be used to lower the 1/f noise.

Appendix B

Wooley 3rd Order Modulator Noise Analysis

Wooley 3rd order Modulator Noise Analysis I

$$Y_1 = \left[\left[\left[\frac{1}{5}X_1 - \frac{1}{5}\cdot Y_1\right]\cdot\frac{1}{3}H_1\right] - \frac{1}{6}Y_1\right]H_2 + Q_1$$

$$Y_1 = \left[\frac{1}{15}X_1H_1 - \frac{1}{15}Y_1H_1 - \frac{1}{6}Y_1\right]H_2 + Q_1$$

$$Y_1 = \frac{1}{15}X_1H_1H_2 - \frac{1}{15}Y_1H_1H_2 - \frac{1}{6}Y_1H_2 + Q_1$$

Common Denominator: 30

$$\frac{30}{30}Y_1 + \frac{2}{30}Y_1H_1H_2 + \frac{5}{30}Y_1H_2 = \frac{2}{30}X_1H_1H_2 + \frac{30}{30}Q_1$$

$$Y_1\left[30 + 2H_1H_2 + 5H_2\right] = 2X_1H_1H_2 + 30Q_1$$

$$Y_1[z] = X_1[z]\cdot\frac{2H_1H_2}{30 + 2H_1H_2 + 5H_2} + Q_1[z]\cdot\frac{30}{30 + 2H_1H_2 + 5H_2}$$

Let $H_1, H_2 = \frac{z^{-1}}{(1 - z^{-1})}$

Simplify $Y_1[z]$: First is the $X_1[z]$ PORTION

$$\frac{\frac{2\,z^{-1}z^{-1}}{(1-z^{-1})(1-z^{-1})}}{30 + \frac{2z^{-1}z^{-1}}{(1-z^{-1})(1-z^{-1})} + \frac{5z^{-1}}{(1-z^{-1})}} \Rightarrow \frac{\frac{2\,z^{-2}}{(1-z^{-1})^2}}{\frac{30\,(1-z^{-1})^2 + 2z^{-2} + 5z^{-1}(1-z^{-1})}{(1-z^{-1})^2}}$$

$$= \frac{2z^{-2}}{30(1-z^{-1})^2 + 2z^{-2} + 5z^{-1}(1-z^{-1})} \Rightarrow \frac{2z^{-2}}{30 - 60z^{-1} + 30z^{-2} + 2z^{-2} + 5z^{-1} - 5z^{-2}}$$

$$= \frac{2z^{-2}}{30 - 55z^{-1} + 27z^{-2}} \Rightarrow \frac{(2z^{-2})\cdot z^2}{(30 - 55z^{-1} + 27z^{-2})\cdot z^2}$$

$$= \boxed{\frac{2}{30z^2 - 55z + 27} \cdot X[z]}$$

Simplify $Y_1[z]$: Second is the $Q_1[z]$ Portion

$$= \frac{30}{30 + \frac{2\cdot z^{-1}z^{-1}}{(1-z^{-1})(1-z^{-1})} + \frac{5z^{-1}}{(1-z^{-1})}} \Rightarrow \frac{30}{\frac{30(1-z^{-1})^2 + 2z^{-2} + 5z^{-1}(1-z^{-1})}{(1-z^{-1})^2}}$$

$$= \frac{30(1-z^{-1})^2}{30(1-z^{-1})^2 + 2z^{-2} + 5z^{-1}(1-z^{-1})} \Rightarrow \frac{30(1-z^{-1})^2}{30(1-2z^{-1}+z^{-2}) + 2z^{-2} + 5(z^{-1}-z^{-2})}$$

$$= \frac{30(1-z^{-1})^2}{30 - 60z^{-1} + 30z^{-2} + 2z^{-2} + 5z^{-1} - 5z^{-2}} \Rightarrow \frac{30(1-z^{-1})^2}{(30 - 55z^{-1} + 27z^{-2})}$$

$$= \frac{30(1-2z^{-1}+z^{-2})}{(30 - 55z^{-1} + 27z^{-2})} \Rightarrow \frac{30 - 60z^{-1} + 30z^{-2}}{(30 - 55z^{-1} + 27z^{-2})} \cdot \frac{z^2}{z^2}$$

$$= \boxed{\frac{30z^2 - 60z + 30}{30z^2 - 55z + 27} \cdot Q_1[z]}$$

Put $X[z]$ & $Q_1[z]$ terms together:

$$\boxed{Y_1[z] = \frac{2}{30z^2 - 55z + 27} \cdot X[z] + \frac{30z^2 - 60z + 30}{30z^2 - 55z + 27} \cdot Q_1[z]}$$

Now to analyze the second portion of the 2-1 architecture

First, we need an expression for U_1:

$$U_1 = \left[\left[\left[\frac{1}{5}X_1 - \frac{1}{5}Y_1\right]\frac{1}{3}H_1\right] - \frac{1}{6}Y_1\right]H_2$$

$$U_1 = \frac{1}{15}X_1H_1H_2 - \frac{1}{15}Y_1H_1H_2 - \frac{1}{6}Y_1H_2$$

$U_1 = Y_1 - Q_1$ so $Y_1 = U_1 + Q_1$

$$U_1 = \frac{1}{15}X_1H_1H_2 - \frac{1}{15}H_1H_2(U_1+Q_1) - \frac{1}{6}H_2(U_1+Q_1)$$

$$U_1 = \frac{1}{15}X_1H_1H_2 - \frac{1}{15}H_1H_2U_1 - \frac{1}{15}H_1H_2Q_1 - \frac{1}{6}H_2U_1 - \frac{1}{6}H_2Q_1$$

$$U_1 + \frac{1}{15}H_1H_2U_1 + \frac{1}{6}H_2U_1 = \frac{1}{15}X_1H_1H_2 - \frac{1}{6}H_2Q_1 + \frac{1}{15}H_1H_2Q_1$$

$$U_1[30 + 2H_1H_2 + 5H_2] = 2X_1H_2H_1 - 5H_2Q_1 + 2Q_1H_1H_2$$

$$U_1[30 + 2H_1H_2 + 5H_2] = 2X_1H_2H_1 + Q_1[2H_1H_2 - 5H_2]$$

$$\frac{U_1}{X} = \frac{2H_1H_2}{30 + 2H_1H_2 + 5H_2} + \frac{Q_1[2H_1H_2 - 5H_2]}{30 + 2H_1H_2 + 5H_2}$$

$$\frac{U_1}{X}[z] = \frac{2}{30z^2 - 55z + 27} \cdot X[z] + \frac{7 - 5z}{30z^2 - 55z + 27} \cdot Q_1[z]$$

Solve for Y_2

$$Y_2 = \left[\frac{3}{4} \cdot U_1 - \frac{1}{20} Y_1 - \frac{1}{5} Y_2\right] H_3 + Q_2$$

$$Y_2 = \frac{3}{4} H_3 \cdot \frac{2}{30z^2 - 55z + 27} \cdot X[z] + \frac{3}{4} \frac{H_3 \cdot [7-5z]}{30z^2 - 55z + 27} \cdot Q_1[z]$$

$$- \frac{1}{20} H_3 \frac{2}{30z^2 - 55z + 27} X[z] - \frac{1}{20} H_3 \frac{30(z-1)^2}{30z^2 - 55z + 27} \cdot Q_1[z]$$

$$- \frac{1}{5} Y_2 H_3 + Q_2$$

Let $H_3 = 1 / (z-1)$, Let common denominator be 20

$$Y_2 + \frac{1}{5} \cdot \frac{1}{(z-1)} \cdot Y_2 = \frac{5 \cdot 3}{5\ 4} \cdot \frac{2}{30z^2 - 55z + 27} \cdot \frac{1}{(z-1)} \cdot X[z] + \frac{3 \cdot 5 \cdot [7-5z]}{5 \cdot 4 (30z^2 - 55z + 27)(z-1)} \cdot \frac{1}{Q_1}$$

$$- \frac{1}{20} \cdot \frac{2}{30z^2 - 55z + 27 (z-1)} \cdot \frac{1}{} \cdot X[z] - \frac{1}{20} \cdot \frac{30(z-1)^2}{30z^2 - 55z + 27 (z-1)} \cdot \frac{1}{} \cdot Q_1[z] + Q_2$$

$$Y_2 [5z \overset{\downarrow}{+4}] = \frac{5 \cdot 3 \cdot 2 \cdot X[z] - 2X[z]}{20 (30z^2 - 55z + 27)(z-1)} + \frac{Q_1 5 \cdot 3 \cdot [7-5z] - 30(z-1)^2 Q}{20 (30z^2 - 55z + 27)(z-1)}$$

$$+ Q_2$$

Solve for Y_2: Continued

$$[5z-4]\cdot Y_2[z] = \frac{28\cdot X[z]}{20(30z^2-55z+27)(z-1)} + \frac{(75-15z-30z^2)\cdot Q_1[z]}{20(30z^2-55z+27)(z-1)} + Q_2[z]$$

$$Y_2[z] = \frac{28\cdot X[z]}{20(30z^2-55z+27)(z-1)(5z-4)} + \frac{(75-15z-30z^2)Q_1[z]}{20(30z^2-55z+27)(z-1)(5z-4)} + \frac{Q_2[z]}{5z-4}$$

Solve for output: $W_1 = z^{-1} = 1/z$, $W_2 = 4(1-z^{-1})^2 = 4(z-1)^2/z^2$

$$Y_{out} = Y_1W_1 - Y_2W_2$$

$$Y_{out} = \frac{2\cdot X[z]\cdot 1}{(30z^2-55z+27)(z)} + \frac{30z^2-60z+30}{(30z^2-55z+27)(z)}\cdot\frac{1}{1}\cdot Q_1[z]$$

$$- \frac{28\cdot X[z]\cdot 4\cdot(z-1)^2}{20(30z^2-55z+27)(z-1)(5z-4)(z^2)} - \frac{(75-15z-30z^2)Q_1[z]}{20(30z^2-55z+27)(z-1)(5z-4)}\cdot\frac{4(z-1)^2}{(z^2)}$$

$$- \frac{Q_2[z]\cdot 4(z-1)^2}{(5z-4)(z^2)}$$

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