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### Size-Dependent Behavior and Challenges in Ag/Al<sub>2</sub>O<sub>3</sub>/Au Memristors: An Investigation into Miniaturization Effect

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Washington University in St. Louis

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JAMES MCKELVEY SCHOOL OF ENGINEERING

**Fall 2023 MEMS 400 Independent Study**

Size-Dependent Behavior and Challenges in Ag/Al<sub>2</sub>O<sub>3</sub>/Au Memristors:

An Investigation into Miniaturization Effect

Principal Investigator: Dr. Sang-Hoon Bae

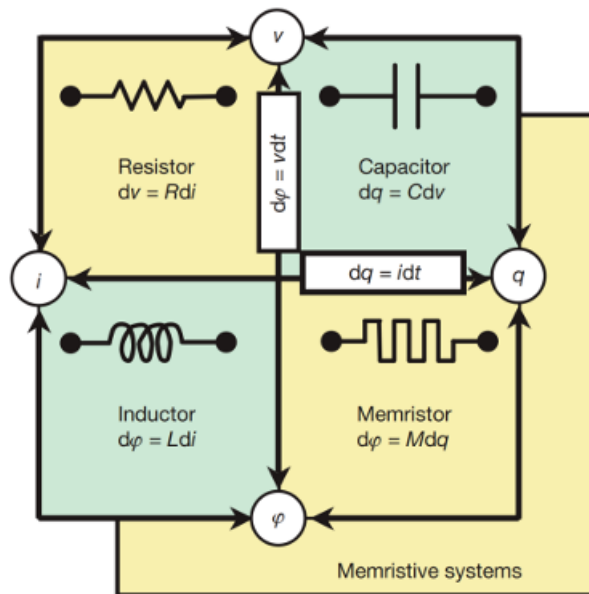
Student: Qingge Catherine Huang

## ABSTRACT

This study investigates the performance of Ag/Al<sub>2</sub>O<sub>3</sub>/Au memristors, focusing on devices with dimensions ranging from 400nm to 1μm. It was observed that smaller devices (400nm and 600nm) consistently display Ohmic behavior, lacking a high-resistance state. This is attributed to increased current density and potential structural imperfections during fabrication. In contrast, larger devices (800nm and 1μm) exhibit volatile threshold switching (VTS) and a notable delay in transitioning from high to low resistance states. The study suggests that this delay is due to the instability of conductive filaments in smaller volumes. Additionally, these larger memristors show short retention of memristive qualities, with consecutive testing leading to breakdown, likely due to Joule heating effects enhancing ionic drift and diffusion. This study underscores the critical influence of device size on metal conductive filament memristor performance, highlighting the challenges in device miniaturization.

## INTRODUCTION

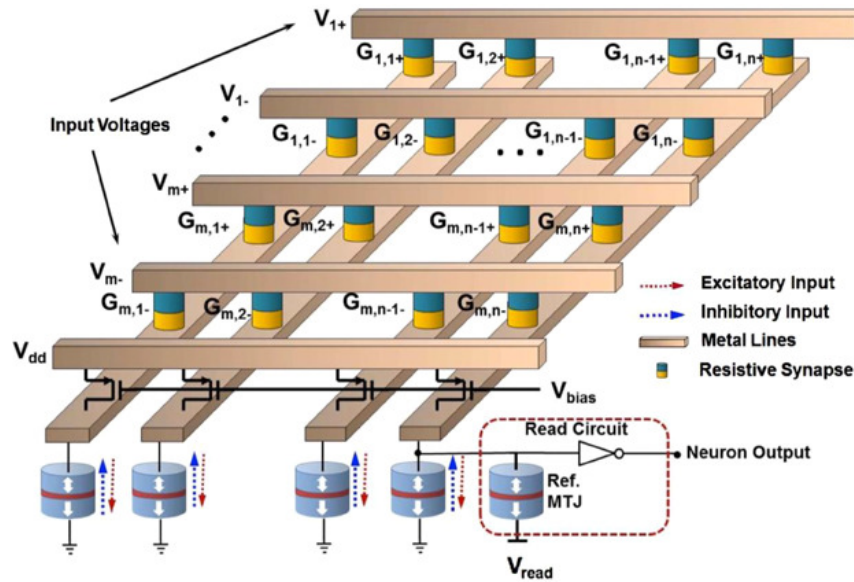
A memristor, short for memory resistor, is a two-terminal circuit element first envisioned by Professor Leon Chua in 1971. In the paper “Memristor–The Missing Circuit Element,” he wrote that this device “has every right to be as basic as the three classical circuit elements already in existence, namely, the resistor, inductor, and capacitor.” [1] These three devices have been known to link the fundamental circuit variables – current  $i$ , charge  $q$ , voltage  $v$ , and flux  $\phi$  – through the following relationships:  $dv = Rdi$ ,  $d\phi = Ldi$ ,  $dq = Cdv$ , supplementing the intrinsic definitions of  $d\phi = vdt$  and  $dq = idt$ . Chua proposed that a memristor, characterized by a relationship between  $\phi$  and  $q$ , should theoretically complete the four quadrants of the basic circuit devices. Chua further demonstrated the possibility of a non-linear resistor changing its resistance value according to its input current or voltage with an active circuit device.



**Figure 1 Passive Basic Circuits and Their Relationships to Circuit Elements [2]**

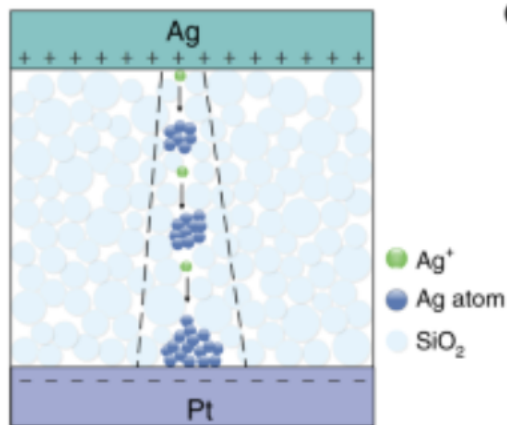
The physical realization of a passive memristor was first completed at the Hewlett Packard laboratory in 2008.[2] This memristor exploits the oxygen vacancy in doped  $TiO_2$ , modulating the resistance value by moving the oxygen vacancy from one electrode to the other via input current. This successful demonstration of the passive resistance switching effect has attracted extensive research efforts. Many memristive devices have been invented based on different design principles. In the age of neuromorphic computing, its potential application in memory sensing and/or computing could significantly reduce energy consumption and transfer speed in data transfer.

In general, the physical realization of a memristor uses the metal/insulator/metal or metal/semiconductor/metal structure, where the insulator and semiconductor should be good ion conductors, such as oxides, sulfides, or organic compounds. Large-scale application of memristor can be realized by integrating each device into a crossbar array, as illustrated below [3]:



**Figure 2 Memristor Crossbar Array**

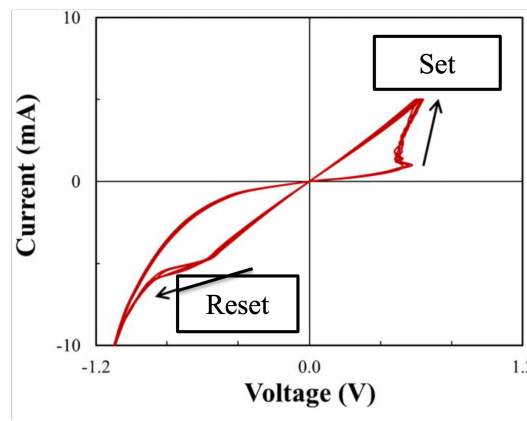
In this independent study, a memristor with the structure  $Ag/Al_2O_3/Au$  was designed, fabricated, and analyzed. The device should exhibit memristive characters based on the filamentary mechanism. When a bias is applied to the active electrode Ag, the metal will be oxidized to Ag ions, which will move towards the inert electrode under the influence of the electric field. During the ion migration process, Ag ions will gradually be reduced, forming a conductive metallic filament in the functional layer material, which transforms the device from a high resistive state to a low resistive state. This process can be seen illustrated below [4]:



**Figure 3 Filamentary Formation in Memristor**

As we gradually increase the voltage applied to the device, we should observe an abrupt change

in device resistance. The voltage at which the device transitions to a low-resistance state is called “set voltage” ( $V_{set}$ ), indicating conductive filament formation. Ideally, after the device has been “set,” we can gradually decrease the applied voltage into the negative domain (opposite direction) and observe the low resistivity state maintains till a certain voltage at which the device switches back to the original high-resistance state. The bias is increased again till it returns to 0V, during which the device keeps at a high resistivity. This process is called voltage “sweeping” and can reveal many qualities about the memristor. The following figure shows a typical I-V curve of a memristor in a shape called ”pinched hysteresis.”[5]

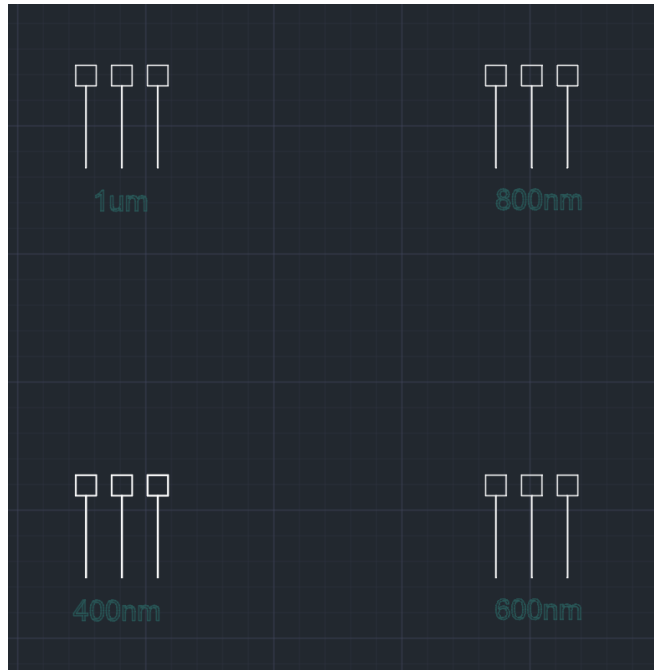


**Figure 4 Typical Voltage-Current Curve of a Memristor**

## METHODS

**Design and Fabrication.** The performance of a memristor depends on its material property and the specific structure. For this study, the insulating material  $Al_2O_3$  was selected as the functional layer material. It is also highly stable due to its strong ionic-covalent bonding and densely packed crystal structure, which provides the basis for its thermal stability and high breakdown voltage. The electrical properties of  $Al_2O_3$  can be finely tuned through doping or controlling its thickness and structure. In addition,  $Al_2O_3$  is compatible with standard semiconductor manufacturing processes, which could potentially reduce the cost and complexity of the production.

The top and bottom electrode was designed in AutoCAD, as shown below in Fig.5. Each electrode pad was 200um by 200nm. The numbers (400nm, 600nm...) indicated the line thickness of the electrodes.



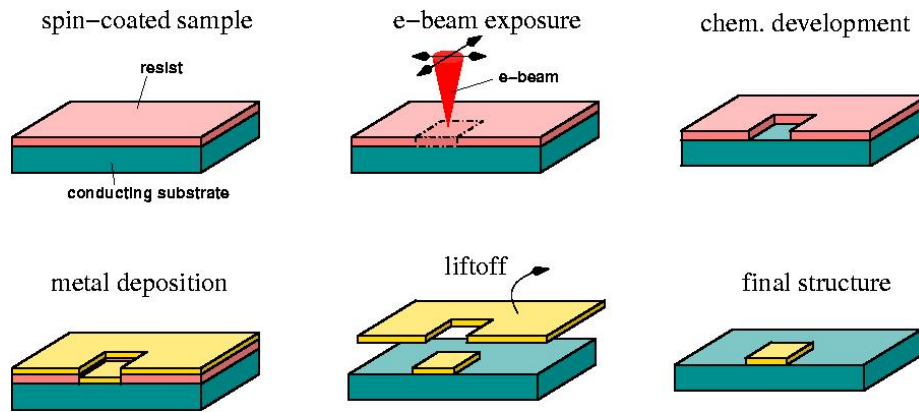
**Figure 5 CAD Drawing of Device Electrodes**

The deposition of the bottom Au electrodes was completed using Electron Beam Lithography (EBL) and Electron Beam Evaporator. A layer of photoresistive PMMA e-beam resist was spin-coated onto the Si/SiO<sub>2</sub> substrate. It underwent soft baking at 180 degrees Celsius to remove the solvents and firmly adhere the polymer layer to the substrate. The layer was then exposed to a focused electron beam, which altered PMMA's structure precisely at the location of the design patterns. During the development process, the area of exposed PMMA was removed by submerging the substrate in a Methyl isobutyl keton (MIBK) solution. PMMA here was used as a positive resist.

The substrate was then cleaned and placed in an electron beam (e-beam) evaporator. The evaporation chamber was evacuated to a high vacuum. A high-energy electron beam was generated using an electron gun, which was directed at the gold material. The gold particles were then evaporated due to the intense energy from the electron beam and condensed to form a thin film on the cooler substrate.

After the formation of a gold thin film across the substrate surface, the device was placed in a beaker with acetone, which lifted off the unwanted parts of Au by dissolving the underlying PMMA.

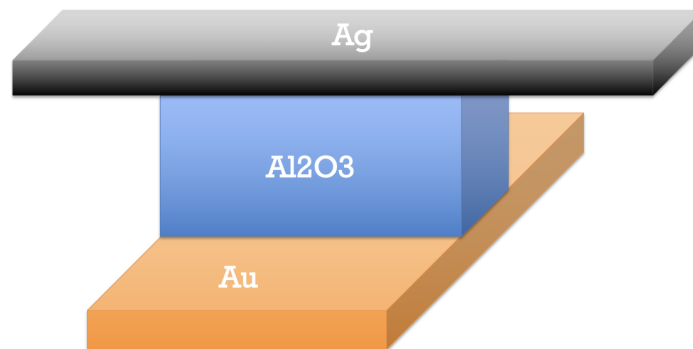
The EBL process is illustrated below [6].



**Figure 6 Electron Beam Lithography Process**

After the deposition of the bottom electrode, the functional layer of  $Al_2O_3$  was deposited via Atomic Layer Deposition (ALD). The method involves the reaction of Trimethylaluminum (TMA) and water on the substrate surface, a chemical process that produces  $Al_2O_3$ . After placing the substrate into the vacuum chamber, TMA was pulsed into the chamber, where it reacted with the substrate surface and formed a layer of aluminum-containing molecules. Excess TMA and reaction byproducts were purged out of the chamber. Water vapor was then introduced, reacting with the treated surface to form a layer of  $Al_2O_3$  (releasing methane as a byproduct). The cycle was repeated multiple times to allow for controlled growth of an  $Al_2O_3$  thin film.

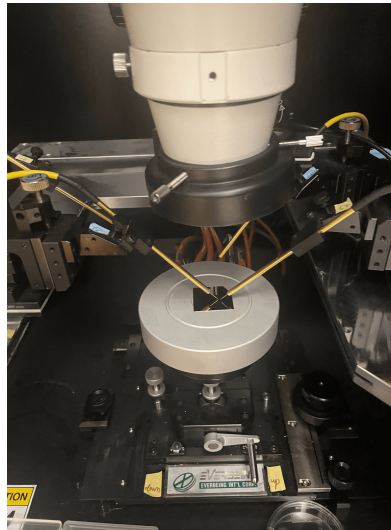
The deposition of the top electrodes was a similar process to the deposition of the bottom ones. Four 3 by 3 cross-bar structures were completed with dimensions from 400nm to 1um, with one memristor located at each intersection. The structure of each memristor is shown below:



**Figure 7  $Ag/Al_2O_3/Au$  Memristor Structure**



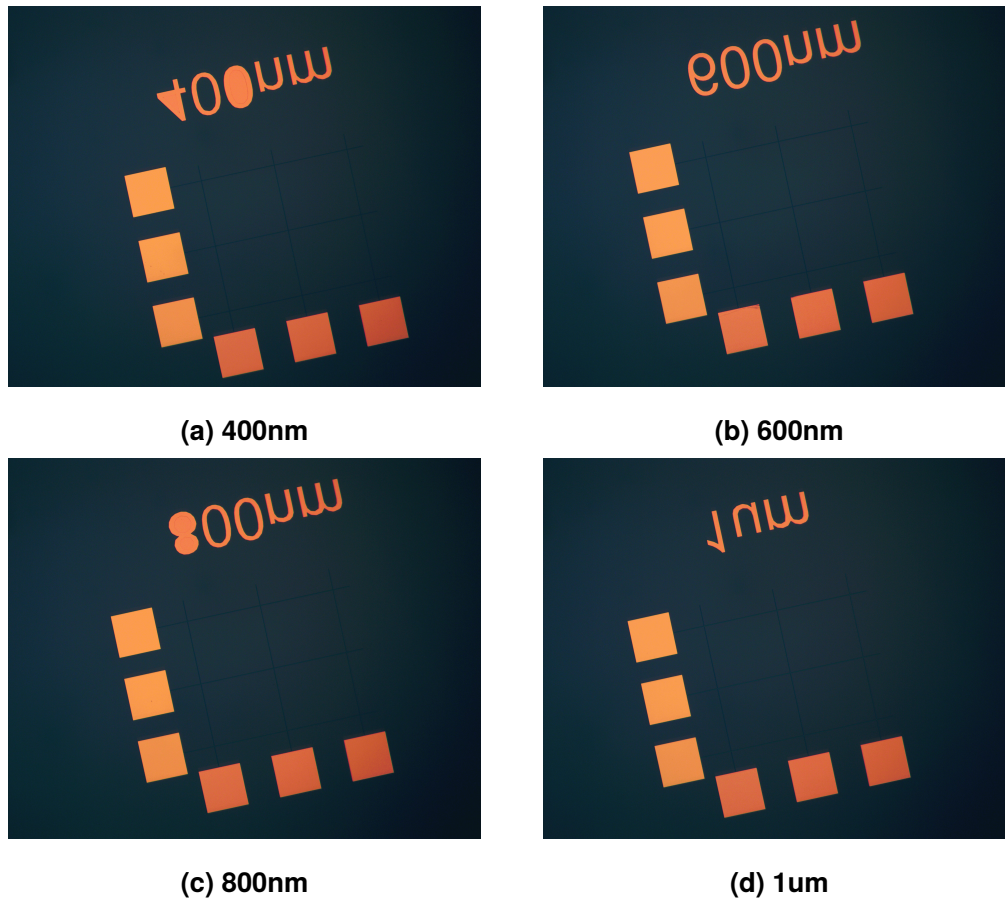
**Device Characterization.** Device characterization involves the use of a probe station and a semiconductor analyzer. The completed memristor was placed onto the probe station platform. Two fine-tipped probes were guided to be in contact with a set of top and bottom electrode pads with the help of an optical microscope. The semiconductor analyzer then applied a sweeping voltage signal to the memristor and the current response was recorded. Multiple tests were conducted for each device to characterize its repeated performance. The following figure is a picture of the probe station used in the study.



**Figure 8 Probe Station**

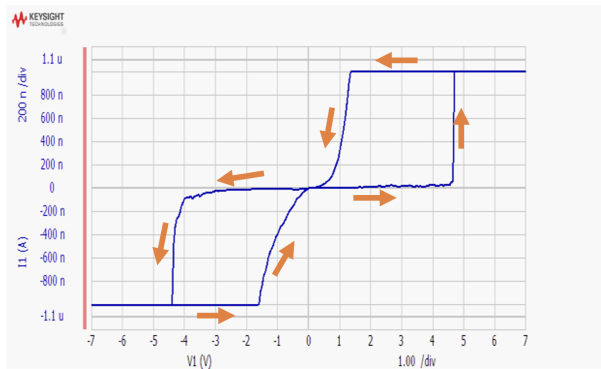
## **RESULTS & DISCUSSION**

The following are optical microscope images of the fabricated memristor cross-bar structures.

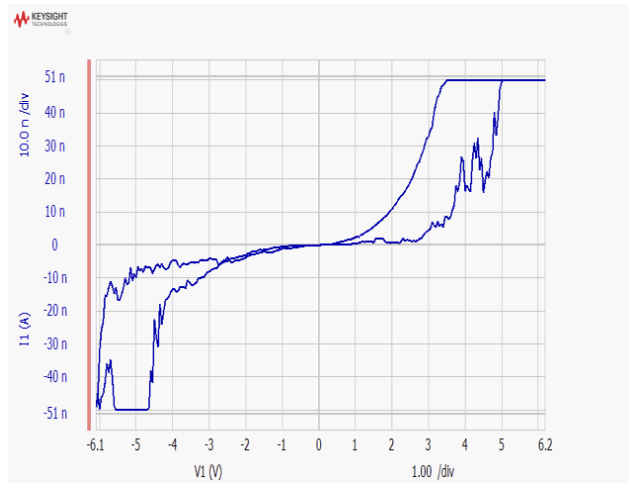


**Figure 9 Device OM Image**

In this study, the materials of the electrodes and functional layer, as well as the thickness of each layer were controlled, so that the device performance could be optimized to the device's cross-sectional area. The following figures are representative of the two types of memristive behavior observed in these devices. Notably, current values in Fig.10 plateaued at certain values, a consequence of the compliance current (CC) setting, which serves a protective function, preventing a current surge that could potentially lead to overheating and subsequent breakdown of the device during the set process.



(a) Dimension=1µm x 1µm; CC=1µA



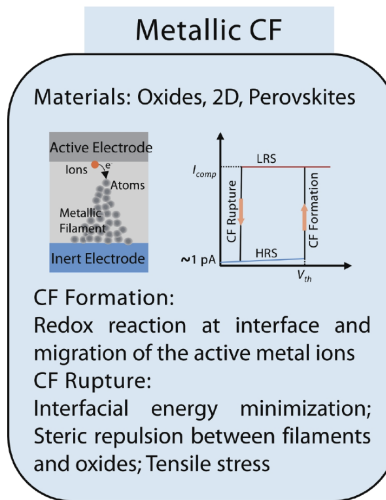
(b) Dimension=800nm x 800nm; CC=50nA

**Figure 10 Representative Setting Behavior**

For 1µm-by-1µm memristors, as shown in Fig.10a, when a sweeping voltage from -7V to 7V is applied to the two electrodes, a low resistance state (LRS) can be observed as indicated by a sudden increase in current. The setting voltage is consistently between 5 and 6V, though it's unable to accurately determine  $V_{set}$  due to the narrative curve behavior during the device's transition to a low resistance state. The reversal of setting voltage causes the device to revert to the high-resistant state (HRS) as the voltage decreases to 0 and goes into the negative region. At a certain negative voltage, it can be observed that the device switches back to LRS. Increasing the voltage back up to zero returns the device to HRS.

In the examination of 800nm-by-800nm and 1µm-by-1µm memristors, two distinct types of setting behavior have been observed. For a subset of these devices, when a sweeping voltage ranging from -7V to 7V is applied across the electrodes, a transition to a Low Resistance State (LRS) is observed, marked by a significant increase in current. The setting voltage, where this transition occurs, consistently falls between 5 and 6V. However, pinpointing the exact setting voltage ( $V_{set}$ ) presents challenges due to the non-linear curve behavior during the device's transition to LRS. Notably, as the voltage diminishes to 0, the slope of the I-V curve gradually increases till the curve is tangent to the x-axis at  $V=0$ , indicating a switch to High Resistance State (HRS), which sustains into the negative voltage domain. At a specific negative voltage, a notable switching back to LRS is observed. Subsequently, increasing the voltage back to zero induces a return of the device to HRS.

This behavior differs from the typical pinched hysteresis curve typically associated with a memristor, particularly in how the device reverts to the HRS within the positive voltage domain. This phenomenon has been identified as volatile threshold switching (VTS). The term “threshold switching” refers to the sharp transition in resistivity that occurs when a certain threshold voltage is reached, while the descriptor “volatile” pertains to the spontaneous rupture of conductive filaments once the external electric field is decreased or removed. The spontaneous rupture is commonly attributed to the diffusion of metal atoms across the contact surface, a process driven by the minimization of interfacial energy between the active electrode, in this case, silver (Ag), and the dielectric  $Al_2O_3$  layer, as reviewed by Zuo et al.[7]



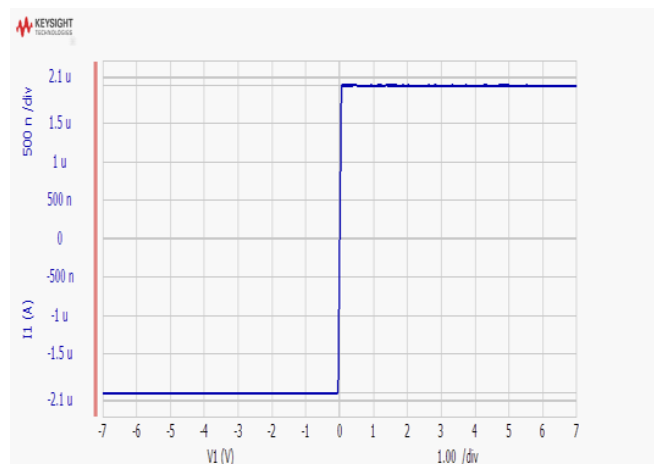
**Figure 11 Volatile Threshold Switching Behavior in Metal Filament Memristor**

For 800nm-by-800nm devices, there are more difficulties in setting the device. The memristors are more prone to break down and become fully Ohmic after just 1-2 attempts, even when subjected to maximum sweeping voltages below their anticipated setting thresholds. (This inference is drawn from the observation that the current remains significantly below the compliance current threshold.) A subset of these memristors that retains memristive behavior also displays VTS, suggesting a filament formation and rupture mechanism akin to that observed in 1 $\mu\text{m}$  devices. However, a notable distinction between the 800nm and 1 $\mu\text{m}$  memristors lies in the breadth of the voltage range over which the transition from HRS to LRS occurs, or more specifically, the extended delay time in the 800nm devices, seen in Fig.10b. This phenomenon suggests that the smaller memristors require a more prolonged application of the electric field to facilitate the switch to LRS. This extended delay could

potentially be attributed to the instability of conductive filaments within the more confined volume of the smaller devices.

Additionally, the devices retain their memristive qualities only for a short amount of time. In the case of 1 $\mu$ m-by-1 $\mu$ m devices, it has been observed that consecutive testing over two to three rounds, without changing any of the testing parameters and within a span of a few minutes, typically leads to device breakdown. One of the causes for this instability is the effect of Joule heating induced by the substantial magnitude of the currents passing through the device. This heat generation exponentially enhances ionic drift and diffusion, substantially altering the switching dynamics. This exacerbated ionic activity at elevated temperatures leads to a rapid deterioration in the device's integrity.[8]

During the device's measurement, it was observed that the memristors with electrode widths of 400nm and 600nm failed to demonstrate memristive behavior. Instead, their current-voltage (I-V) characteristics adhered to Ohm's Law, exhibited by a linear relationship manifesting as a straight line intersecting the origin of the plot. This observation implies that in the context of Ag/Al<sub>2</sub>O<sub>3</sub>/Au memristors, when the cross-sectional area of the device is relatively small, it lacks a distinguishable high-resistance state. Figure 12 is a representative Ohmic curve for such a device.



**Figure 12 Ohmic Behavior in Memristors with a Small Cross-Sectional Area**

To explain the lack of memristive behavior, one potential explanation is the structural imperfections introduced during the fabrication process, given elevated manufacturing precision is required at 400nm and 600nm. However, the observed consistent low-resistive behavior across the device suggests that the underlying issue may be inherent to their design and structure. The

reduced cross-sectional areas in these smaller devices result in increased current density, which could accelerate the breakdown of  $Al_2O_3$  layer, effectively turning the dielectric layer into a resistive element. Furthermore, the increased current density in smaller device areas will likely generate substantial heat. This increase in temperature could, in turn, accelerate the diffusion of metal ions within the dielectric layer, leading to a more rapid formation of conductive paths. These paths further deviate the device from expected memristive behavior.

**Improvements.** To fully understand the performance observed in this independent study, I suggest that in-situ transmission electron microscopy (TEM) should be conducted. This technique will enable a more detailed characterization of the filament dynamics within the memristor under varying bias conditions and is pivotal for explaining the transition to Ohmic behavior as the device dimensions are reduced. In addition, thickness modulation should be included in the study, as discussed by Prezioso et. al.[9] The layer thickness should be defined during the fabrication process or through Atomic Force Microscopy (AFM). Taking this dimension into account will provide a more comprehensive understanding of the device's behavior. A more qualitative study of the device behavior should involve the comparison between the high and low resistance values in the same device, namely the on-off ratio, which can only be conducted on a select few 1um-by-1um devices in this case.

## CONCLUSION

In conclusion, this study of the performance of  $Ag/Al_2O_3/Au$  memristors reveals a clear correlation between metal conductive filament memristors' dimensions and their behavior. Smaller memristors predominantly exhibit Ohmic characteristics, likely due to increased current density and potential fabrication challenges. Conversely, larger memristors demonstrate volatile threshold switching and delayed transitions between resistance states, with their memristive properties rapidly degrading under consecutive testing. Improvements to the study can be made with in-situ microscopy, thickness modulation, as well as qualitative study to better understand the switching dynamic of the memristor. The findings underscore the complexities in memristor miniaturization and highlight the need for balanced stability and functionality in nano-scale memristors.

## References

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# A Raw Data Plots

Below are the raw data plots for the 1 $\mu$ m and 800nm devices.

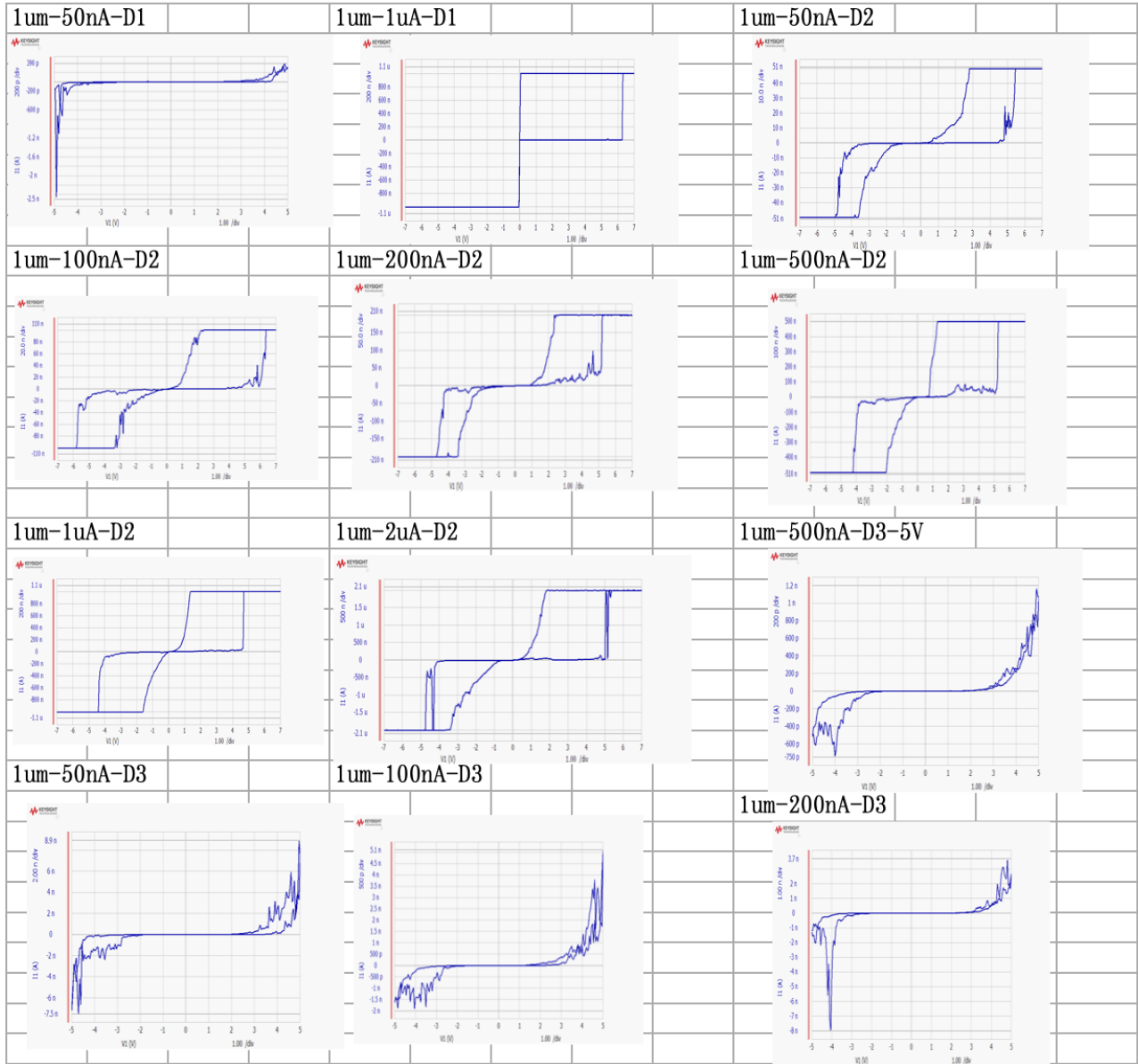
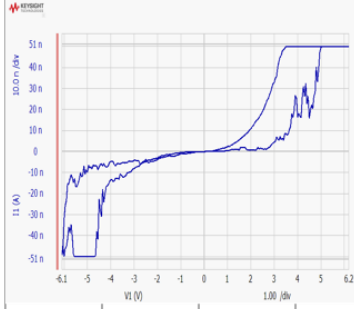


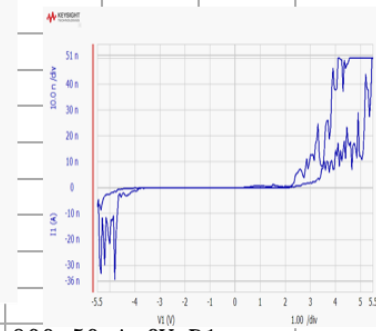
Figure A.1 1 $\mu$ m Raw Data



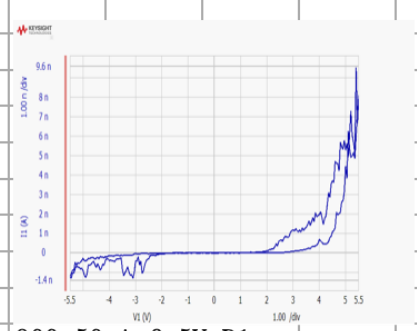
800-50nA-6. 2V-D1



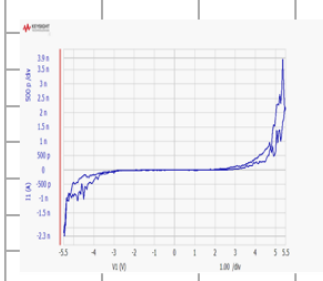
800nm-50nA-5. 5V-D1



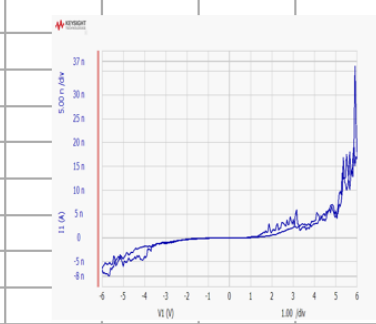
800-100nA-5. 5V-D1



800-500nA-5. 5V-D1



800-50nA-6V-D1



800-50nA-6. 5V-D1

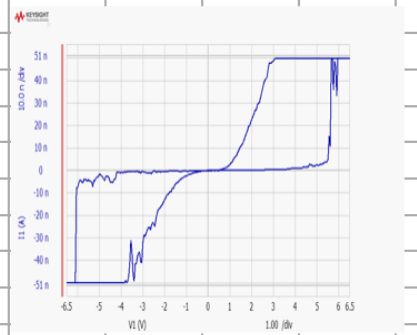


Figure A.2 800nm Raw Data