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Fundamentals of microfluidics fabrication process and the machining of hollow micropillar array

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Abstract

This report firstly introduces the fundamental knowledge of microfabrication which will be used in producing micropillar array, such as photolithography, physical vapor deposition, lift-off and reactive ion etching. Then by using different instruments to do microfabrication, which involves four main steps: lift-off, etching holes from backside of wafer, etching holes from frontside of wafer and etching pillars from frontside of wafer. The details of these four steps will be shown in this report. Next, the outcome will be discussed by comparing the difference between designed micropillar dimensions and real micropillar dimensions. Afterward, the main drawback of this experiment is also discussed and figure out how to solve this problem. Finally, the future work also be mentioned in this report.

1. Introduction

1.1 Background of microfabrication

Microfabrication has been developed for several decades and it has become one of the most promising methods in all kinds of filed [1], e.g., biosensing [2-3], drug delivery [4-5], nanotube [6-7] and fluid dynamic analysis [8-9].

In this report, the fundamentals of some basic microfabrication processes (thermal oxidation, spin coating, sputtering, and reactive ion etching) were studied, the microfabrication of micropillar array were performed in cleanroom, and at last, the characterization of the fabrication samples were performed to quantify the fabrication quality.

1.2 Fundamentals of microfabrication process

1.2.1 Oxidation of Silicon

Silicon oxide is widely used in microfabrication process as insulation layers and passivation layers due to its extremely low electrical conductivity and high chemical resistance. There are several methods to growth silicon dioxide on wafers, and the most promising method is thermal oxidation.

For thermal oxidation on silicon wafers, it can usually be divided into three: wet oxidation, dry oxidation and pyrogenic oxidation (Figure 1.1). Wet and dry oxidation involve heating of a silicon in wet or dry oxygen/nitrogen mixtures at temperatures between $600\,^{\circ}C$ and $1250\,^{\circ}C$ in a quartz furnace. Pyrogenic oxidation uses oxygen, nitrogen and hydrogen to generate ultrapure steam at temperatures between $600\,^{\circ}C$ and $1250\,^{\circ}C$ in a quartz furnace.
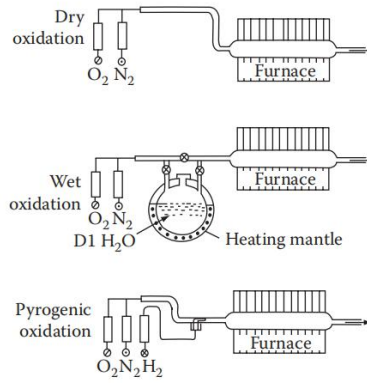
Figure 1.1 Schematic drawing of three different Oxidation method: dry oxidation, wet oxidation, and pyogenic oxidation [10]

Compared with wet oxide, dry oxide grows more slowly. However, the oxide layers are more uniform. In wet oxide, water molecules will decompose hydrogen atoms, which degrade the oxide quality. But a major advantage of wet oxide is the faster growth rate, make it useful for thick layer's oxidation. The reactions of wet and dry oxidation are shown as follows:

$Si + 2H_2O(gas) \rightarrow SiO_2 + H_2$ (wet oxidation)   Reaction 1.1

$Si + O_2(gas) \rightarrow SiO_2$ (dry oxidation)   Reaction 1.2

For pyrogenic oxidation, the gas hydrogen generates ultrapure steam, which helps to remove impurities by volatizing any metal impurities.

There are three steps in gas-phase oxidation processes: gas-phase oxidant moves to the surface of wafer, gas diffuses through the surface of oxide and the oxidation reaction. Figure 1.2 shows the relationship between silicon dioxide thickness and growth time.
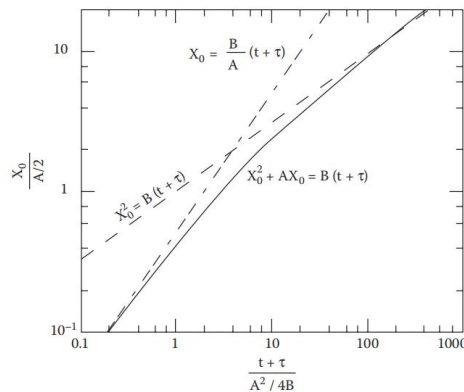

Figure 1.2 Silicon dioxide thickness versus growth time. [10]

For thin oxides, the reaction rate is limited by:

$$X_{ox}(t) = \frac{B}{A}(t + \tau) \tag{1.1}$$

For thick oxides, the reaction rate is limited by:

$$X_{ox}(t) = \sqrt{B(t + \tau)} \tag{1.2}$$

Where A, B and τ are strong functions of temperature, strong functions gas ambient and weak

functions of orientation and doping.

1.2.2 Photolithography

Photolithography is widely used in IC industry and other microfabrication fields. The main processes of photolithography contain: (1) spin coating, (2) photoresist deposition, (3) soft baking (removal of solvent and built-in stresses), (4) exposure, (5) postexposure treatment (improvement on the adhesion) and (6) development. Next, the report will mainly introduce three important processes: spin coating, exposure of photoresist and development.

1.2.2.1 Spin Coating

In photoresist deposition, spin coating is one of main methods of deposition. Spin coating is the first step in the lithography process. Firstly, a wafer is held on a vacuum chuck. Then a thin layer of photoresist which is sensitive to UV radiation is deposited on the oxide surface (see Figure 1.3). The photoresist is dispensed onto the wafer by a speed of about 500 rpm. Finally, to thin the photoresist thickness to the desired thickness, the step range from 1500-6000 rpm will be used.
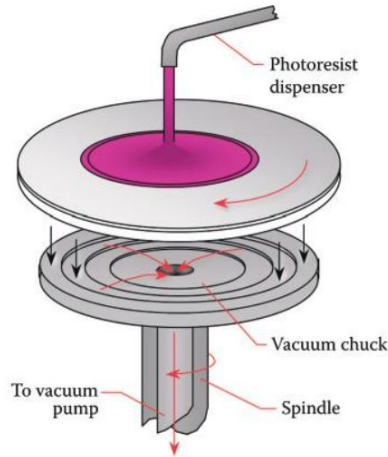

Figure 1.3 Schematic drawing of the spin coating. [10]

For spin speed T, the empirical expression for T is given by:

$$T = \frac{KC^{\beta}\eta^{\gamma}}{\omega^{\alpha}}$$

(1.3)

Where K = the overall calibration constant

C = the polymer concentration in g/100-mL solution

η = the intrinsic viscosity

ω = the number of rotations per minute

Table 1.1 shows some spin coating troubleshooting:

Table 1.1 Spin Coating Troubleshooting Chart [10]

Film too thin	Solution
Spin speed too high	Select lower speed
Spin time too long	Decrease time during high-speed step
Film too thick	**Solution**
Spin speed too low	Select higher speed
Spin time too short	Increase time during high speed step
Exhaust volume too high	Adjust exhaust lid or house exhaust damper

1.2.2.2 Photoresist

The photoresists are mainly made of a polymer, a sensitizer and a casting solvent. The polymer changes structure when exposed to UV light. The solvent allows form a even and thin layer on the wafer surface. The sensitizers control the chemical reactions in the polymeric phase.

There are two types for photoresist, positive and negative. For positive resist, exposed polymer will be weak by breaking their chains, so it will be soluble in development. For negative resist, exposed polymer becomes stable by linkage of main chains, so it becomes less soluble in development. (Figure 1.4).
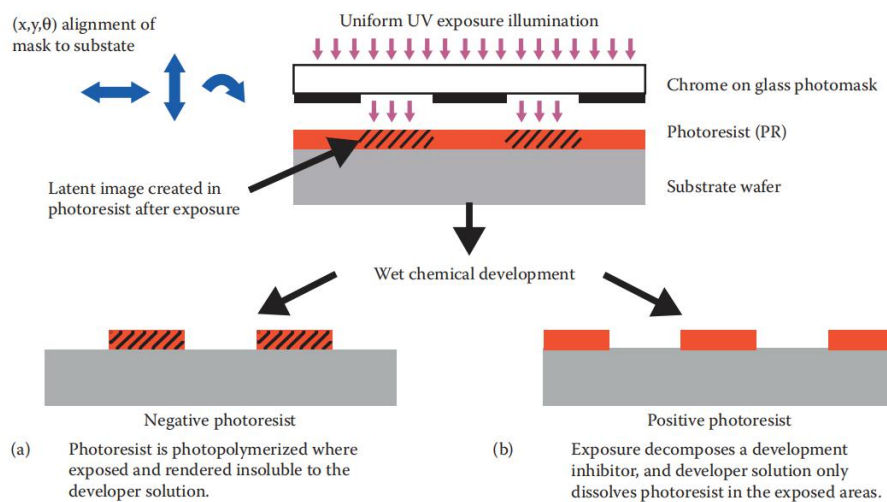

Figure 1.4 Positive and negative resist, after exposing: (a) Negative resists remain in the exposed region. (b) Positive resists develop in the exposed region. [10]

Negative resists are highly resistant to acid and alkaline aqueous solutions. So, it is more chemically resistant than positive resist. This resistance ensures better retention of features during a long etch. Negative resists also are more sensitive than positive resists. However, it has lower contrast. A comparison of negative and positive resists is shown in Table 1.2.

Table 1.2 Comparison of Negative and Positive Photoresists

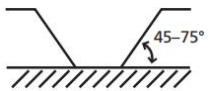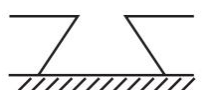| Characteristic	Resist Type	
	Positive Resist	Negative Resist
Adhesion to silicon	Fair	Excellent
Contrast	Higher	Lower
Cost	More expensive	Less expensive
Developer	Temperature sensitive	Temperature insensitive
Liftoff	Yes	Yes
Resolution	High	Low(>1μm)
Thermal stability	Good	Fair
Wet chemical resistance	Fair	Excellent
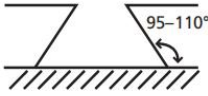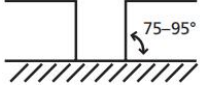
1.2.2.3 Development

Development is a process which dissolves unpolymerized resist to form image. There are two main technologies for development: wet development and dry development.

Positive resists are mainly developed in aqueous alkaline solutions, negative resists are developed in organic solutions. There are also some drawback, for example, the aqueous development rate will be influenced by pH of the developer and the temperature, what's more, the organic solvents lead to swelling of the resist and loss of adhesion.

In general, after development, three different photoresist wall profiles may be obtained as shown in Table 1.3. For positive resists, undercut profile is desired for liftoff, but it's not good for plasma etching. Vertical profile is good for liftoff and reactive ion etch. Normal or overcut is typical for wet etch. For negative photoresists, undercut profile is normal.

Table 1.3 Photoresist Profile [10]

Profile	Dose	Developer Influence
Positive resists undercut 95–110°	High	Low
Positive resists vertical 75–95°	Normal	Moderate
Positive resists normal or overcut 45–75°	Low	Dominant
Negative resists undercut	Dominant	Little influence

1.2.3 Physical Vapor Deposition

Many thin films in microfabrication are deposited by evaporation and sputtering, both are physical vapor deposition (PVD). Mostly, PVD is used to deposit metals. PVD has main three steps: (1) the formation of vapor from the source material; (2) transport the vapor to the substrate of wafer. (3) deposit the vapor onto the surface of the wafer.

One technique of PVD is sputtering, for sputtering, the substrate is under substrate holder (anode) and the target material at cathode side. The target (a disc of the material to be deposited) is bombarded with positive argon ions which created in a plasma. The neutral atoms of target material is sputtered by momentum transfer, and deposited onto the substrate placed on the anode. Figure 1.6 shows a setup of sputtering.
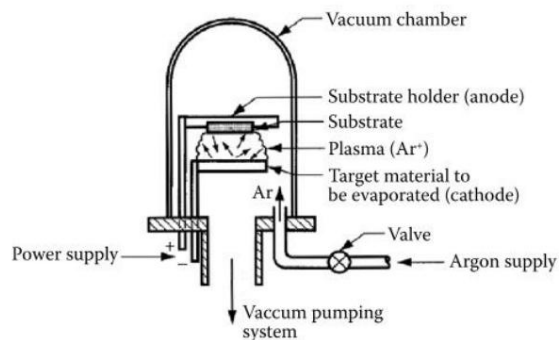

Figure 1.6 Schematic drawing of a PVD chamber. [10]

Compared with thermal evaporation, sputtering has a wider choice of materials for both metallic and

nonmetallic materials, and better film properties (Figure 1.7), such as step coverage. The comparison of thermal evaporation and sputtering is shown in Table 1.4.
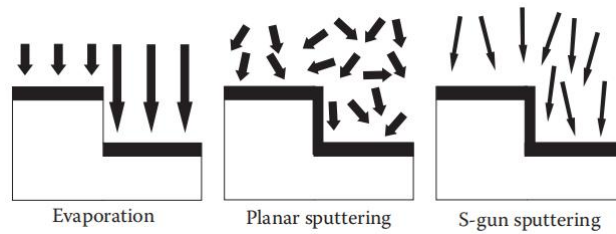

Figure 1.7 Evaporation vs. Sputtering. [10]

Table 1.4 Comparison of thermal evaporation and sputtering [10]

	Evaporation	Sputtering
Choice of materials	Limited	Unlimited
Changes in source material	Easy	Expensive
Uniformity	Difficult	Easy
Thickness control	Difficult	Possible
Adhesion	Poor	Excellent
Film properties	Fewer grain orientations	Many grain orientations

1.2.4 Lift-off

Lift-off method is usually used to form a certainty thin-film metal pattern on the wafer surface. As shown in the Figure 1.8, a photolithograph process must be performed before this step (usually with two photoresist layers). After the development process, metals can be deposited on the wafer surface. After the thin-film deposition, the wafer will be placed in acetone or remover PG to dissolve the remaining photoresist and the unwanted metal pattern will be washed away.
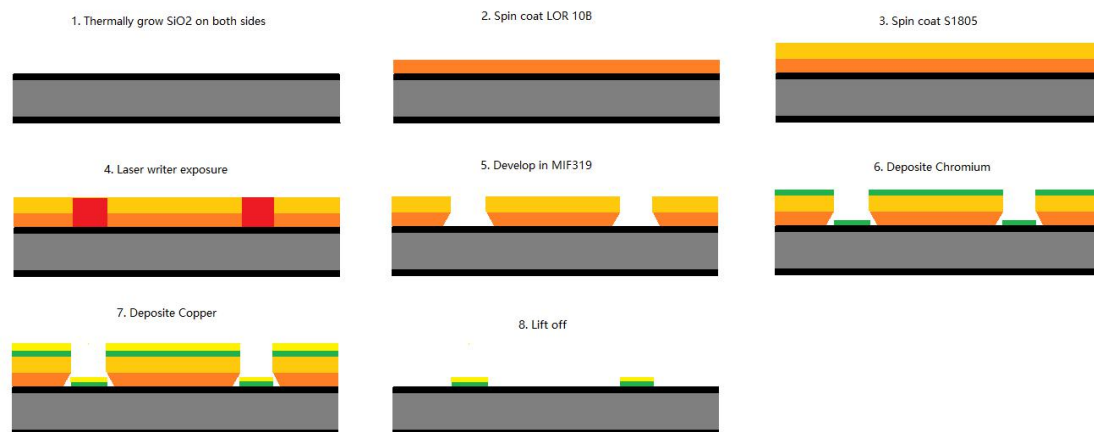

Figure 1.8 Processes of lift-off.

1.2.5 Dry Etching

Dry etching is a technology for etching solid surface. It involves three methods: (1) solid surface is etched in gas or vapor phase by ion bombardment physically, (2) solid surface is etched in gas or vapor phase by chemical reaction at the surface chemically, (3) solid surface is etched in gas or vapor phase by combined physical and chemical methods or reactive ion etching (RIE). The key for dry etching is plasma.

Compared with wet etching, dry etching has several advantages: fewer disposal problems, less undercutting and anisotropic.

1.2.6 Physical/Chemical Etching

Physical/Chemical etching (RIE) could etch solid surface in highly anisotropic etching. Because line-of-sight-impacting ions damage the surface or a passivation layer cleared by the ion bombardment which clear horizontal surfaces only.

1.2.7 Deep Reactive Ion Etching

According to low etch rates and low-aspect ratios for dry etching. Deep Reactive Ion Etching (DRIE) is a very attractive solution. Especially, Robert Bosch GmbH (Stuttgart, Germany) came up with a high-aspect ratio and etch rates process called Bosch process, it solved thermal stresses problem. There are two rotational steps, passivation (C_4F_8) and etching (SF_6), in this process. (see Table 1.5). In the passivation step, a thick fluorocarbon deposits on the surface and form a layer. Then in etching step, energetic SF_x^+ ions remove this layer at the bottom of a trench, as sketched in Figure 1.9.

Table 1.5 Characteristics of DRIE Process

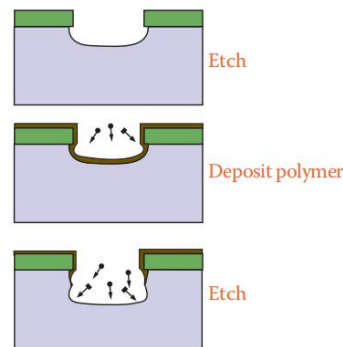|	
SF_6 flow	30-150 sccm
C_4F_8 flow	20-100 sccm
Etch cycle	5-15 s
Deposition cycle	5-12 s
Pressure	0.25-10 Pa
Temperature	20-80 °C
Etch rate	1.5-4 μm/min

Figure 1.9 Illustration of the Bosch process. [10]

1.2.8 Profilometry

Profilometry uses a hard tip moved over a surface with very tiny pressure and simultaneously measures texture and step height. The tip moves on the surface and actuates a linear variable differential transducer that converts movement in electrical signal. The resolution of the height step is about 1 nm. The horizontal resolution depends on tip radius. So, it's better for small tips but it's easier to be damaged by mishandling. Figure 1.10 shows the tip of profilometry.
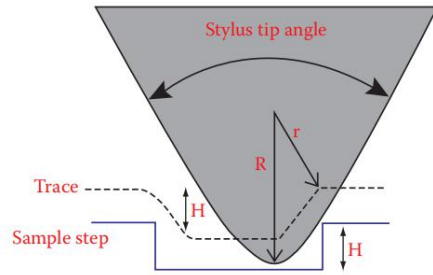
Figure 1.10 Tip of profilometry. [10]

1.2.9 Ellipsometry

Ellipsometry is a noncontact optical technique used for analysis and metrology. In ellipsometry, a sample reflects light and changes the polarization state, and this polarization change is represented by amplitude ratio, ψ, and phase difference, Δ. Then ellipsometry will measure the ratio of two values which depends on optical properties and thickness of materials. So, the thickness of transparent films can be measured. Figure 1.11 illustrates ellipsometry setup.
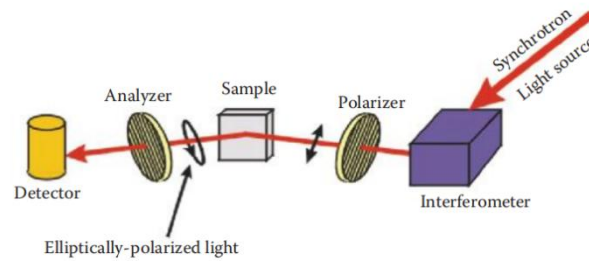

Figure 1.11 Ellipsomeetry setup. [10]

2. Experiment

2.1 Objective

To test evaporation and heat dissipation rate of one kind of micropillar array. This micropillar array need to be done in clean room. Find one 4-inch silicon wafer which both sides are SiO_2 surfaces, set one side as backside and do spin coating on backside, then do photolithography and development. After that deposit Cr on backside and liftoff. Then Bosch process etch SiO_2 and Si on backside to through holes. Next, do photolithography on frontside and use Bosch process to etch SiO_2 and Si to form micropillar structure. Figure 2.1 shows CAD pattern of micropillar array.
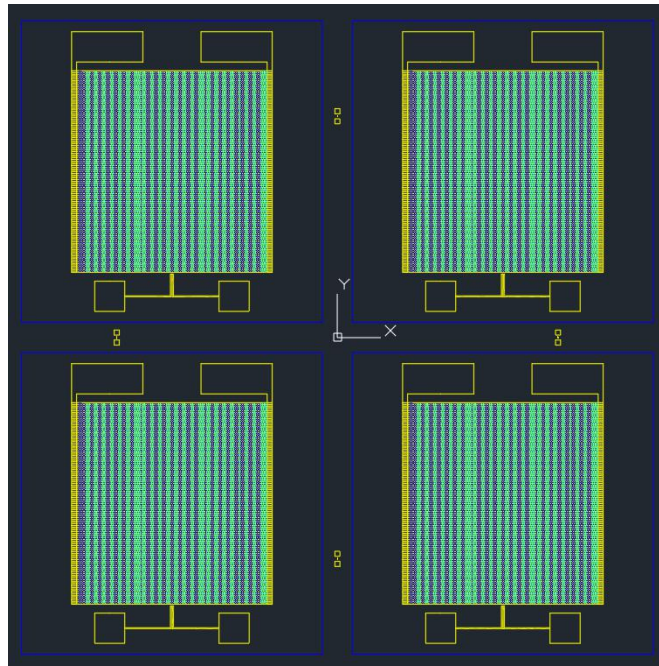
(a)
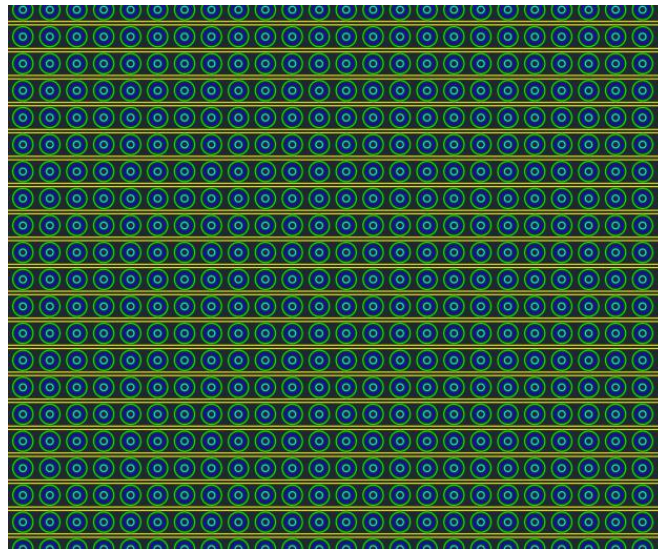
(b)

Figure 2.1 CAD pattern of micropillar array. (a) overall patterns of 4-inch silicon wafer, there are 4 micropillar arrays. (b) micropillar and hole patterns for one micropillar array. Yellow lines are Cr which heat up when apply current. Green circles are micropillars of frontside. Blue circles are holes of backside.

2.2 Micropillar Array Microfabrication Recipe.
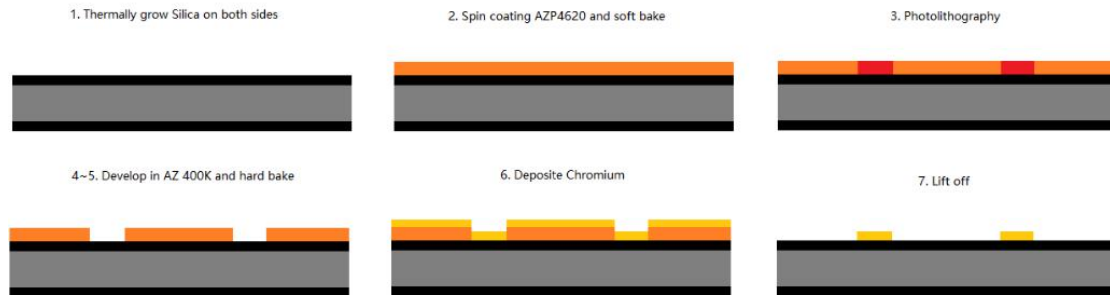
I. Oxidation, Sputtering and Liftoff

Figure 2.2 Flow chart of backside oxidation, sputtering and liftoff.

1. Thermally grow SiO_2 on both sides of silicon wafer for several hours.
2. Spin coating AZP4620 photoresist and soft bake.
3. Photolithography.
4. Develop in AZ 400K.
5. Hard bake.
6. Physical Vapor Deposition of Cr.
7. Lift-off using Acetone.
8. Clean substrate and dry.
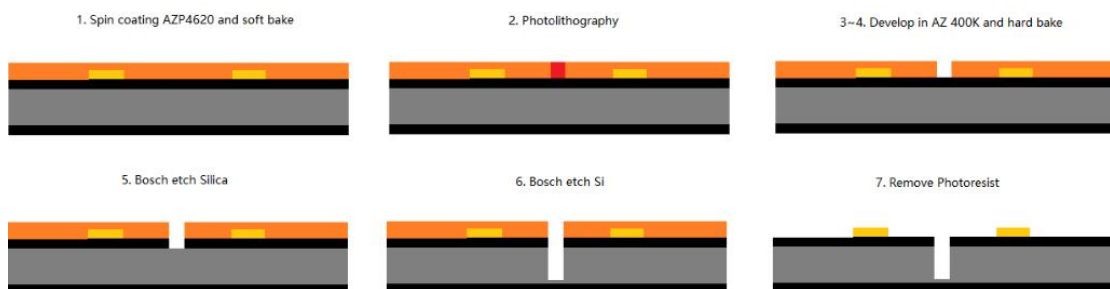
II. Backside through holes

Figure 2.3 Flow chart of backside through hole

1. Spin coating AZP4620 photoresist and soft bake.
2. Photolithography.
3. Develop in AZ 400K.
4. Hard bake.
5. RIE process etches SiO_2.
6. Bosch process etches Si.
7. Remove photoresist in Acetone, clean and dry.

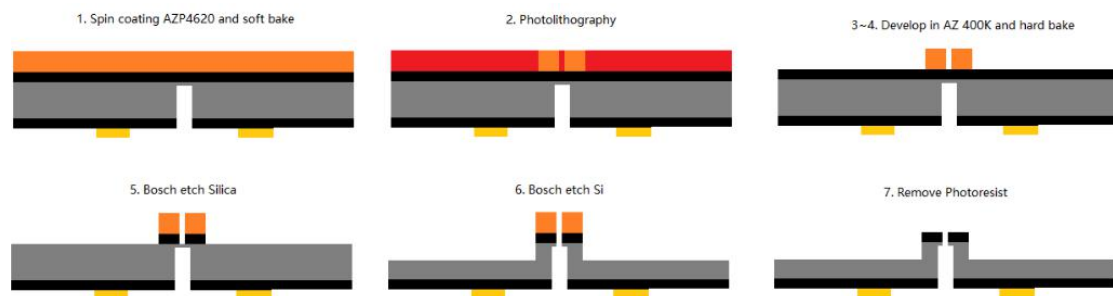## III. Frontside through holes and micropillar

Figure 2.4 Flow chart of frontside through hole and micropillar

1. Spin coating AZP4620 photoresist and soft bake.
2. Photolithography.
3. Develop in AZ 400K.
4. Hard bake.
5. RIE etchs SiO_2.
6. Bosch etch Si.
7. Remove photoresist in Acetone, clean and dry.

2.3 Processes of Microfabrication

2.3.1 Thermal Oxidation

According to requirements of recipe. Thermal oxidation is the first step. In this experiment, use 4-inch silicon wafer, then put it into Lindberg tube furnace (Figure 2.5) and heat up to $1100\,^{\circ}C$ for 18 hours. Finally take the wafer out when the temperature of the furnace decrease to room temperature.

Figure 2.5 Lindberg tube (glass) furnace.

2.3.2 Photolithography

Use acetone, IPA, DI water to wash wafer sequentially. Then use Al foil to cover the internal surface of spin coater. Put wafer on vacuum chuck, calibrate the center of wafer and pour AZP4620 on wafer. Set revolutions per minute (RPM) and duration. After setting, spin and soft bake. Figure 2.6 shows the Brewer Science CEE 200X Spin Coater.

Put wafer on the stage of laser writer when wafer cooled down. Convert CAD drawing into dxf file

and export designs.

For backside sputtering, the processes of operating the laser writer is as follows:

1. Move the wafer under the laser head.
2. Descend the laser head to approach the wafer.
3. Use macro camera to find the center of the wafer.
4. Set focus, intensity and filter.
5. Find design in files.
6. Expose the wafer.

For backside through holes, control of the laser writer as follows:

1. Move the wafer under the laser head.
2. Descend the laser head to approach the wafer.
3. Use macro camera to find alignment marks and do global alignment to calibrate angle of the wafer.
4. Find the wafer center.
5. Use micro camera to do alignment.
6. Set focus, intensity and filter.
7. Find design in files.
8. Expose the wafer.

For frontside through holes and micropillar, control of the laser writer as follows:

1. Move the wafer under the laser head.
2. Descend the laser head to approach the wafer.
3. Use backside macro camera to find alignment marks and do global alignment to calibrate angle of the wafer.
4. Find the wafer center.
5. Use the micro camera to do alignment.
6. Set focus, intensity and filter.
7. Find design in files.
8. Expose the wafer.

After exposure, put wafer into AZ 400K developer. Finally, hard bake. Figure 2.7 is the Heidelberg Laser Writer. Appendix A-1 shows the wafer after developing. Appendix A-4 and A-5 show the backside holes patterns after development.
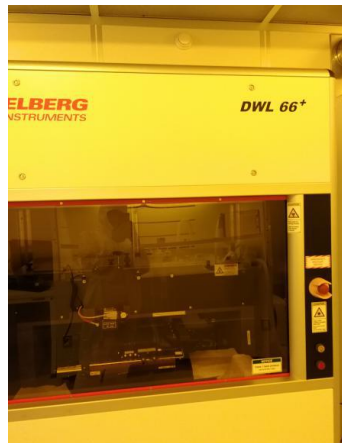

Figure 2.6 Brewer Science CEE 200X Spin Coater.

Figure 2.7 Heidelberg Laser Writer.

2.3.3 Sputtering and Liftoff

For sputtering, use Kurt Lesker PVD 75 Physical Vapor Deposition system (Figure 2.8). The processes of Sputtering are as follows:

1. Open argon and nitrogen gases valves.
2. Vent chamber.
3. Cover plate with Al foil.
4. Stick wafer on the plate.
5. Put the plate in the chamber.
6. Put target into source container.
7. Pump down the chamber.
8. Run recipe.
9. Vent the chamber when finished.
10. Take the plate out and clean the chamber.
11. Pump down the chamber.
12. Turn off the argon and nitrogen gases valves.

Finally, put the sputtered wafer into acetone for 1 hour and clean it (Appendix A-1). Appendix A-2 and Appendix A-3 show two dimensions of wafer after liftoff.

Figure 2.8 Kurt Lesker PVD 75 Physical Vapor Deposition system

2.3.4 RIE

Use Oxford Instrument's Plasmalab System 100 Inductively Coupled Plasma (Figure 2.9) to do RIE. The processes of RIE is as follows:

1. Use Cool Grease to stick the wafer and carrier wafer together.
2. Open C_4F_8 and SF_6 gases valves.
3. Vent chamber.
4. Put wafer on chuck.
5. Evacuate chamber.
6. Run RIE recipe.
7. Vent chamber when finished.
8. Take the wafer out.
9. Evacuate chamber and run clean recipe.
10. Turn off C_4F_8 and SF_6 gases valves.

Appendix A-6 to A-9 show the RIE for backside holes, frontside holes and frontside pillar. Appendix A-10 and A-11 show the frontside wafer and backside wafer after microfabrication.

Figure 2.9 Oxford Instrument's Plasmalab System 100 Inductively Coupled Plasma

3. Results and conclusion

In this project, the main purpose is to use photolithography and RIE to make a micropillar array. The main challenge of this project is how to etch through the wafer and make the dimension as close as possible to the required value. So under these requirements. Set different parameters in both sides and use Bosch processes to etch the holes from both sides, which could solve some problems such as the diameter of holes are too big to meet the requirement if only etch the wafer on single side. And use Bosch processes to etch the wafer could protect the sidewall of the holes from etching. However, the precision will decrease due to deviation of alignment in step of photolithography on two sides. But this drawback could be neglected by calibrating laser writer head's position. Figure 2.10 shows cross-section image of scanning electron microscope (SEM). It shows that our recipe of DRIE is suitable to do etching holes process without extending holes' diameter.

The quality of microfabrication are shown in Appendix from A-12 to A-15. According to Appendix A-12 and A-13, the diameters of the hole and micropillar are larger than designed diameters (frontside holes are 50 μm, micropillars are 100 μm and backside holes are 150 μm). The reason of it maybe because of over development or excessive etch cycles. A-14 and A-15 show a new micropillar with smaller diameter (frontside holes are 40 μm and micropillars are 80 μm). From A-14, it's obvious to see that there are cool grease in some holes. These residues will influence DRIE process sometimes
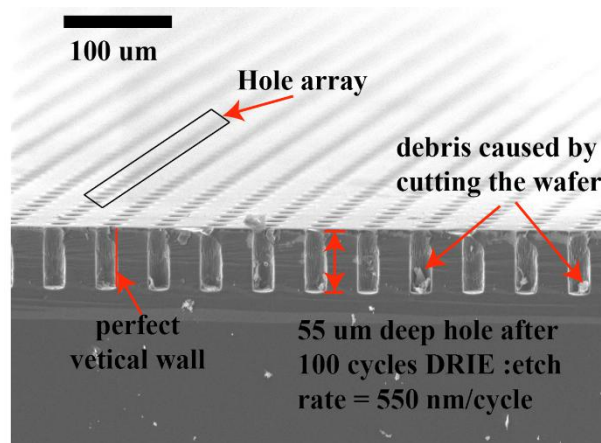
even result in failure of DRIE process.

Figure 2.10 SEM image of micropillar array, there are some residues in holes.

Although there are some small flaw such as the residues of photoresist and cool grease will prevent DRIE from etching, this flaw can be solved by using ultrasonic bath. Anyway, this independent study explored the feasibility of using some methods such as Bosch processes to solve the problem of etching efficiency and accuracy in microfabrication. This report showed that these processes of microfabrication can get an optimistic result, in future, the main goal is to optimize recipe of DRIE to meet different dimensions of micropillar.

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Appendix

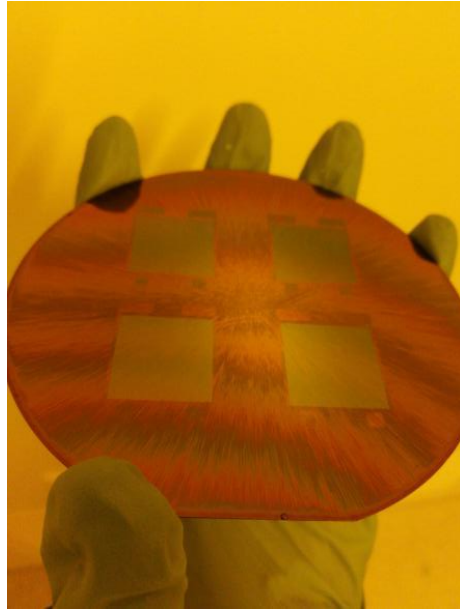A-1 Wafer after liftoff
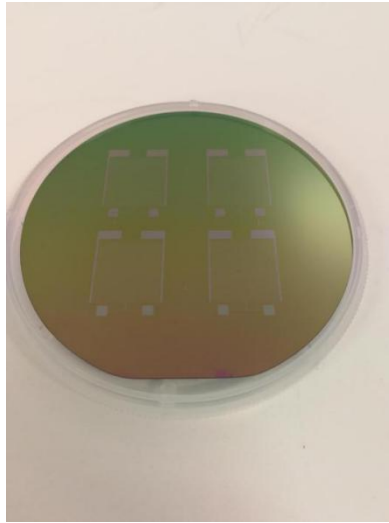
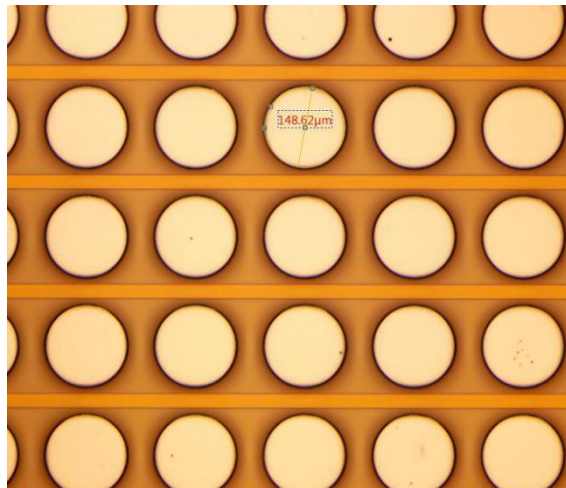A-2 Dimension of deposited pattern after liftoff
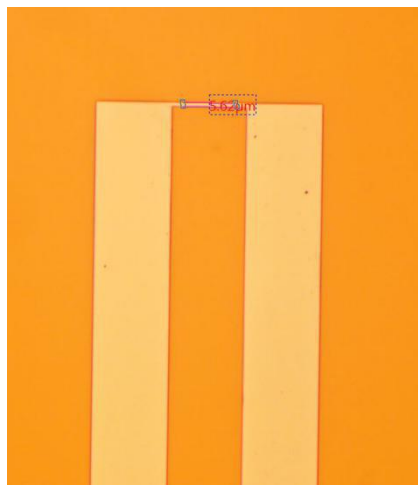
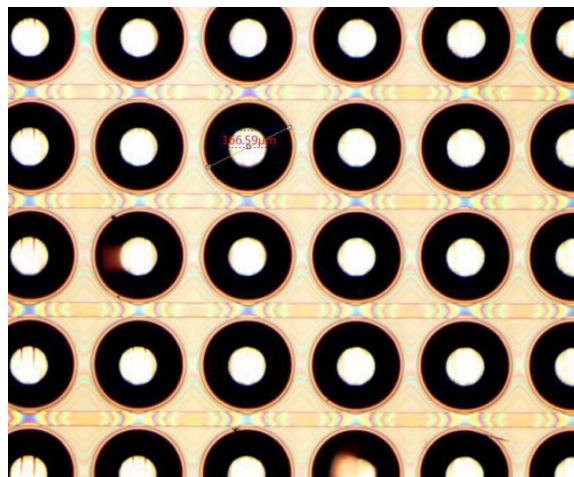A-3 Dimension of deposited patterns after liftoff

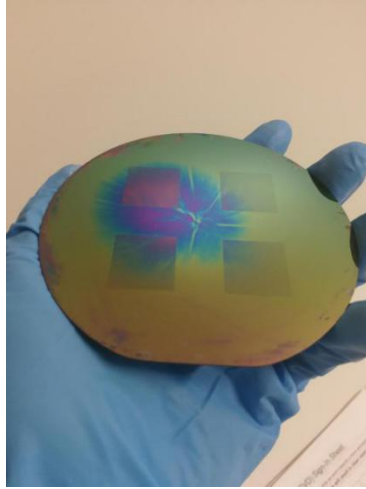A-4 Backside hole patterns after development

A-5 Dimension of backside hole patterns after development
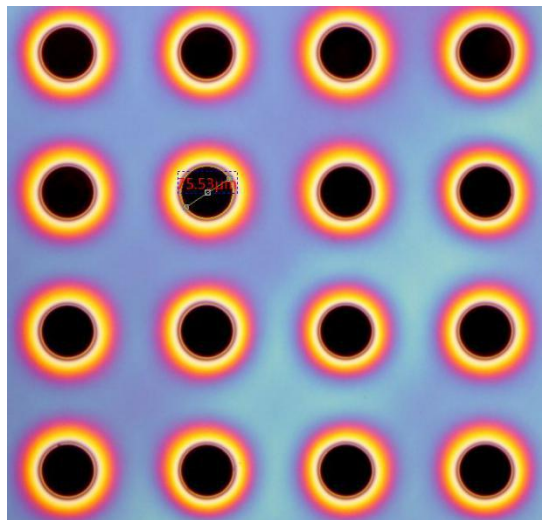

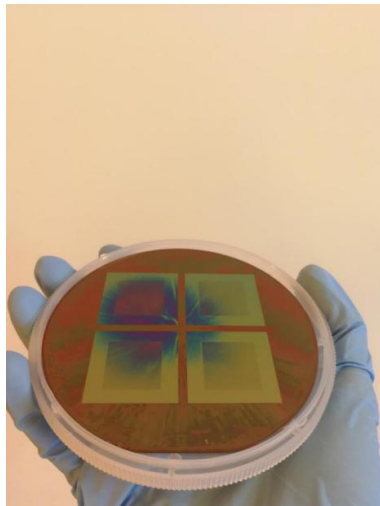A-6 Dimension of backside holes after etching
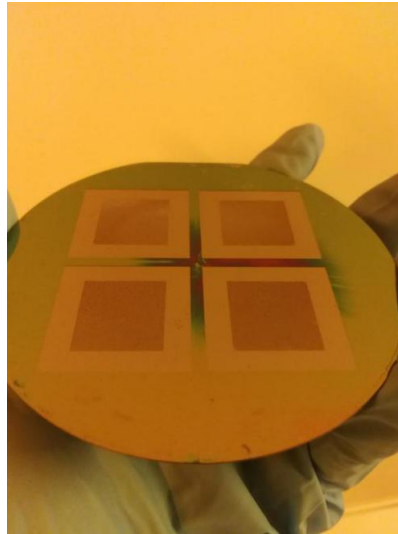
A-7 Wafer after frontside holes etching
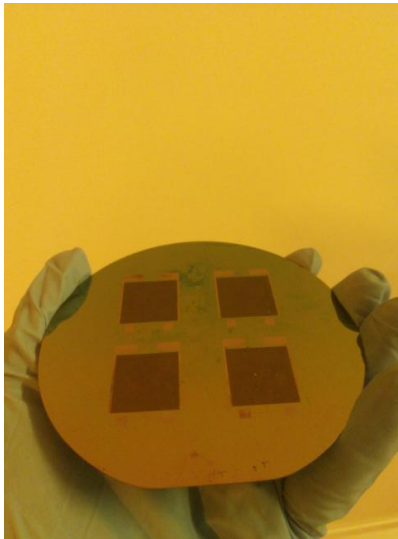

A-8 Dimension of frontside holes after etching
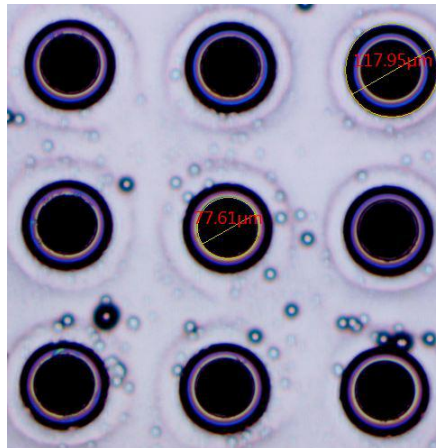

A-9 Wafer after etching micropillars

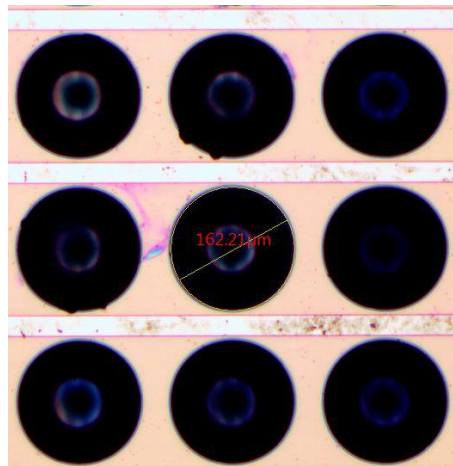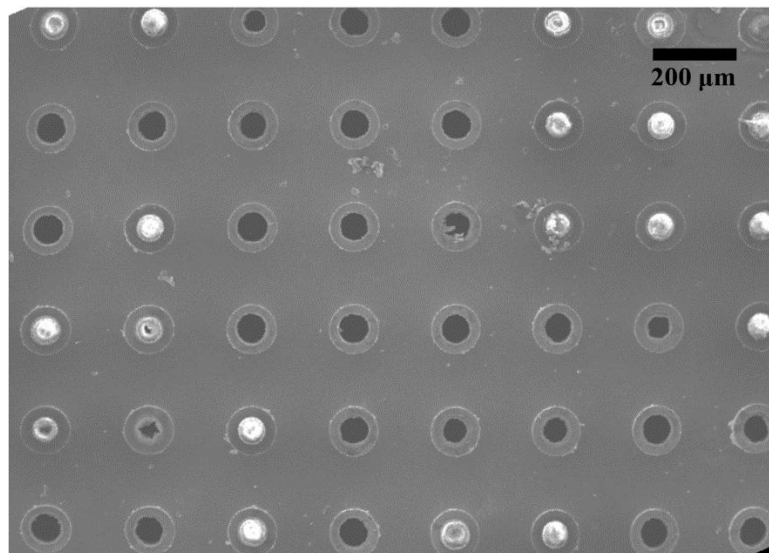A-10 Frontside of wafer

A-11 Backside of wafer

A-12 Dimensions of frontside holes and micropillars

A-13 Dimension of backside holes

A-14 SEM image of micropillar array

A-15 SEM image of one micropillar