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Globally Clocked Magnetic Logic Circuits

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Abstract

Magnetic spin valve devices enable the design of logic and memory elements that are suitable for use when constructing digital systems. A master-slave flip-flop design is proposed that can be clocked using an externally applied global magnetic field. With an external global clock, the digital system no longer needs to deliver the clock on-chip, thereby eliminating the need for a clock distribution network. We assess the power, area, and speed implications associated with the ability to eliminate the clock distribution network on a hybrid CMOS-magnetologic digital system.

1 Introduction

Clock distribution in current integrated circuits can amount to a significant portion of the total area and power consumption of a chip, comprising as much as 40% of chip area [1] and as much as 40% of power consumption [2]. As integration densities increase, these percentages are likely to increase and the problem of clock skew due to variable delays in the clock signals will become more severe. Elimination of the clock distribution network could dramatically reduce on-chip power dissipation, reduce routing complexity, and eliminate clock skew in future integrated circuits. A digital latch which

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is clocked by an externally applied, global signal would enable the clock distribution network to be removed.

We have investigated a magnetic logic device and architecture that uses an externally applied, ac magnetic field as a global clock signal for the circuit. The clock field, applied along the hard axis of the magnetic device, dynamically reduces the switching threshold. This supports the construction of an externally clocked D latch. The addition of another on-chip enabling signal creates an "enabled D latch." The enabled latches can be configured to respond to either a positive or negative clock field, allowing them to be configured as a two-phase master-slave flip-flop appropriate for sequential logic circuits. The structure of each latch is similar to a spin valve MRAM cell [3].

In this paper, we introduce the operation of the enabled D latch and the master-slave flip-flop. In addition, we assess both the viability of the devices and the performance impact of their use in a hybrid CMOS-magnetologic digital circuit.

2 Magnetologic Devices

2.1 Enabled Latch

A MRAM bit cell is fundamentally a D latch. Activation of the word line causes the storage of the bit line data in the magnetic state of the spin valve. We use an identical structure to build the enabled latch with the distinction that an externally applied magnetic field is used in addition to the on-chip generated fields.

As shown in Fig. 1(a), this device therefore has three inputs: data (D), enable (EN), and clock (CLK). Two of these inputs are currents on metal lines that are perpendicular to each other and run across the top of the spin valve. The data line (D) and enable line (EN) generate fields in the easy axis and hard axis directions of the spin valve respectively. In addition, the third input (CLK) is an externally applied bidirectional magnetic field that adds to the hard axis field.

As with a traditional latch, the D input provides the next state on a clock signal with enable active. The EN input in conjunction with the external clock (CLK) enables the latch to be set (essentially by lowering the threshold necessary for the D input to induce a magnetic state change).

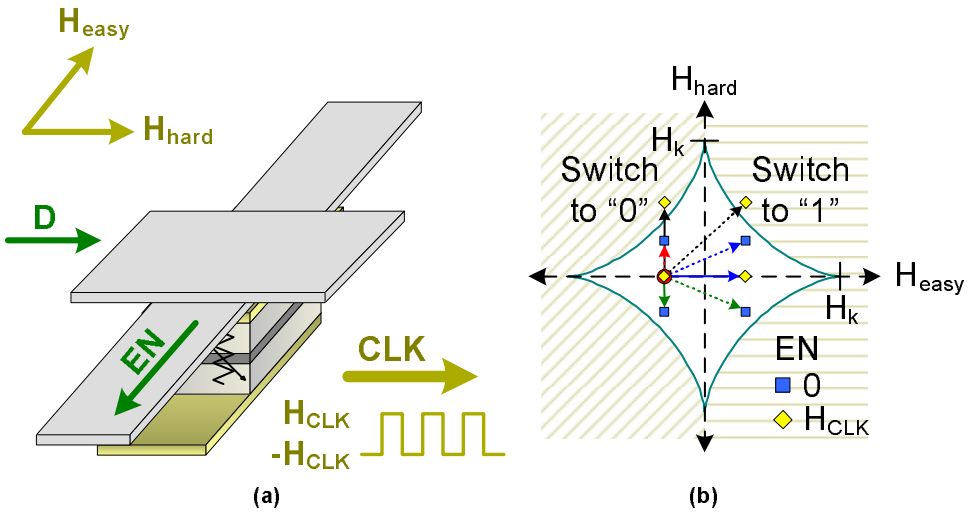

Figure 1: Enabled D latch constructed using a magnetic device. The D input induces a field along the easy axis and is used to set the magnetization state of the top magnetic layer. The EN input induces a field along the hard axis and is perpendicular to the D input.

The Stoner-Wohlfarth switching diagram is shown in Fig. 1(b). The astroid shape is the switching threshold of the spin valve as a function of the field along the easy and hard axes. Applying a sufficiently large field causes the direction of magnetization of the free layer to switch depending on the polarity of the H_{easy} field. In this figure, the convention used is that a positive H_{easy} field will switch the output state to a 1. Likewise, a negative H_{easy} field will switch the output state to a 0. Points within the astroid will not change the magnetic state of the device.

Operation of the latch is illustrated with the Stoner-Wohlfarth switching astroids for the spin valves. The possible magnetic field vectors that can be seen by the spin valve due to the current in the D, EN, and the external bipolar clock field are indicated by the constellation of symbols. To allow unipolar currents in the data line, the easy axis field is offset using an internal bias field in the spin valve. A low current (D = 0) in the data line leaves the net field in the left half of the astroid. A high current (D = 1) makes the net field positive in the easy axis direction. The magnitude of the enable current and external clock field are chosen so that each alone will not result in a field outside of the stable region in the astroid. With enable low, the field can

reach only the square points within the astroid. Only when the clock is on and enable is on can the field in Fig. 1(b) exceed the switching threshold (the top two diamonds) and switch the magnetic state of the latch according to the current value of the D input.

2.2 Optimal Offset and Signal Field Levels

A fixed offset can be induced along the easy axis of the latch during fabrication that allows the D input to use unidirectional current pulses. The reliability of the latch to switch according to the Stoner-Wohlfarth switching diagram in Fig. 1(b) depends on the noise margin of the device which is measured as the distance from the operating point to the switching threshold. According to Stoner-Wohlfarth theory the switching boundary is given by:

$$H_{easy}^{p} + H_{hard}^{p} = H_{k}^{p} \qquad \text{where } p = \tfrac{2}{3} \tag{1}$$

and H_k is the anisotropy field. Based on this, an optimal offset can be found that maximizes the noise margin of the device. To find this optimal dc offset, we first solve Eqn. 1 for H_{hard}. This gives us an equation for the switching threshold of the device:

$$H_{hard} = \left(H_{k}^{p} - H_{easy}^{p}\right)^{\frac{1}{p}} \tag{2}$$

Then, the equation of a line perpendicular to H_{hard} can be calculated:

$$\begin{aligned} m_{\perp} &= -1/\left(\frac{dH_{hard}}{dH_{easy}}\right) = H_{easy}^{1-p} \cdot \left(H_{k}^{p} - H_{easy}^{p}\right)^{1-\frac{1}{p}} \\ b_{\perp} &= H_{hard} - m_{\perp} \cdot H_{easy} \\ y &= m_{\perp} x + b_{\perp} \end{aligned} \tag{3}$$

This gives the following line equation:

$$y = H_{easy}^{1-p} \cdot \left(H_{k}^{p} - H_{easy}^{p}\right)^{1-\frac{1}{p}} \cdot (x - H_{easy}) + \left(H_{k}^{p} - H_{easy}^{p}\right)^{\frac{1}{p}} \tag{4}$$

Solving for H_{easy} as a function of a point (x, y) will give the closest point along the Stoner-Wohlfarth switching astroid to (x, y). Given the points (H_{easy}, H_{hard}) and (x, y), where H_{hard} was previous defined in Eqn. 2, the distance between them can be calculated:

$$d(x, y) = \sqrt{\left(H_{easy}(x, y) - x\right)^{2} + \left(H_{hard}(x, y) - y\right)^{2}} \tag{5}$$

In Eqn. 5, x represents the magnetic field strength along the easy axis, which corresponds to the dc offset we seek, and y represents the magnetic field strength along the hard axis. For the latch in Fig. 1, there are two fields along the hard axis that add. Setting the strength of these fields to s, we can find an s such that $d(x, s) = d(x, 2s)$.

The noise margin becomes $d(x, s)$. The optimum offset for a given field strength is found by maximizing this function.

2.3 Master-Slave Flip-Flop

A master-slave flip-flop is one of the basic register circuits used in a synchronous digital system. It is formed from two enabled transparent latches connected in a master-slave topology. CMOS circuitry is used to transition from the output of the master device to the input of the slave device. Fig. 2 (top) shows how to build such a flip-flop using magnetologic devices. Here, two magnetologic latches, as previous described, are shown with their enable lines connected together forming a "U" shape. Consequently, a current into the page on the enable input of the master latch gives a current out of the page in the slave latch. This allows the two latches to operate on opposite phases of the clock. Since the global external clock is common to all devices on a chip, the devices are oriented such that the hard axis is in the same direction as the clock field.

The external clock is bidirectional, applying a positive (H_{CLK}) and negative ($-H_{CLK}$) field along the hard axis. The possible field vectors seen by the master and slave spin valves are illustrated in the Stoner-Wohlfarth switching diagrams of Fig. 2 (bottom) by the constellation of symbols. For the master latch, the field generated by a positive current pulse in the enable line is equal to $-H_{CLK}$. When the clock is low, it supports this field with an additional $-H_{CLK}$ field which exceeds the switching threshold and changes the magnetization state of the device. Likewise, for the slave latch, the field generated by the enable line is equal to H_{CLK} which, when supported by the additional H_{CLK} field generated by a high clock, will exceed the switching threshold.

This flip-flop has an advantage over traditional CMOS master-slave designs which are susceptible to errors if the two clock polarities are not correctly phase aligned. Since the proposed magnetic latch is clocked by a single bipolar clock, it cannot experience clock skew between phases of the clock.

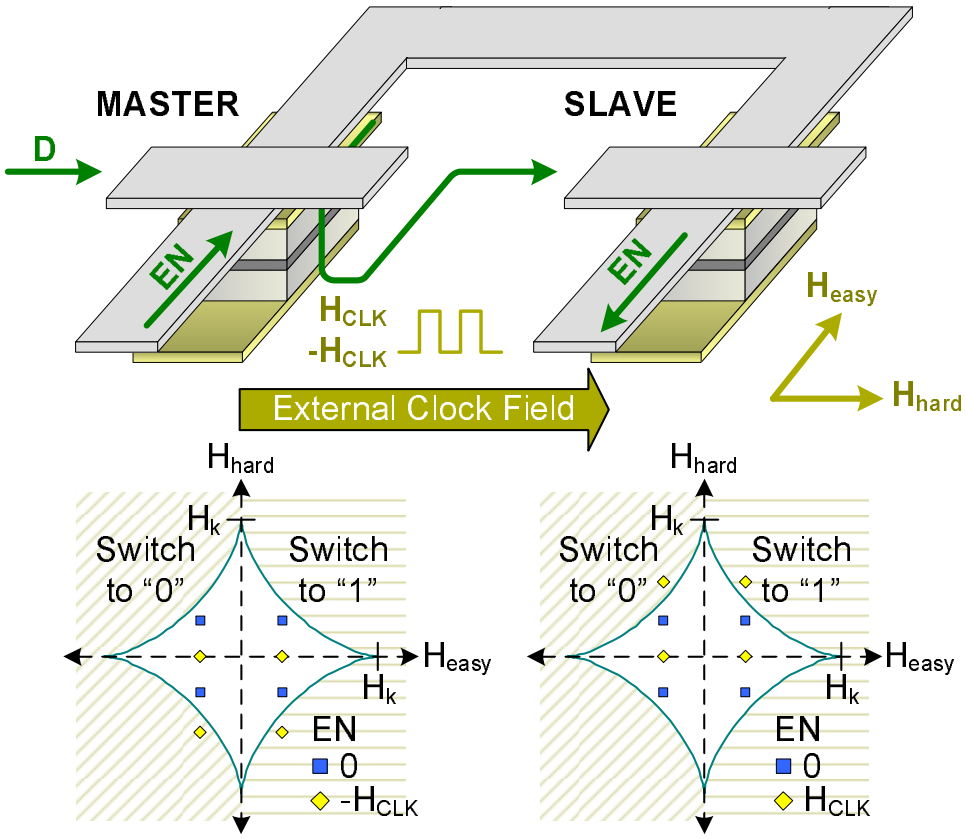

Figure 2: Enabled master-slave flip-flop constructed using two magnetologic latches. The D input is applied to the master latch, which is loaded when EN is active and CLK is low. When CLK goes high, the output of the master latch sets the value of the slave latch.

3 Viability

The viability of the proposed logic architecture using externally clocked magnetic latches is founded on existing MRAM technology. Switching astroids such as those shown if Fig. 1(b) have been measured in spin valves using crossed write lines as in Fig. 1(a) [3] and are found to closely match the classic Stoner-Wohlfarth model. The process for integration of such devices with standard CMOS circuits is now well established and already used in commercial MRAM products. Matsunaga et al. demonstrated the combination of embedded magnetic latches in a CMOS logic circuit [4]. They also

provide a comparison between their hybrid CMOS-magnetologic design and traditional CMOS in terms of area and power, showing similar area requirements and lower power requirements with a 0.18 μm CMOS process. It should be noted, however, that they are using the newer spin-torque transfer devices [5], which limits the ability to do direct power comparisons with the field-induced switching devices considered here.

A similar approach incorporating the proposed externally clocked, enabled latch should not be technologically more difficult. Thereby, the output state of the master flip-flop can be sensed using CMOS electronic circuits, and applied to the data line of the slave flip-flop. The connection from the slave to the following master is made in a similar fashion, potentially combined with other signals in combinational logic gates.

Ideally, one would like to dispense with the CMOS circuitry altogether and directly connect the output of one latch to the input of the other. However, despite recent advances in tunneling magnetoresistance technology, the best on:off resistance ratios of current spin valve devices are still only about 2:1, making it difficult to achieve sufficient changes in output current, with magnetic logic devices alone, to reliably switch a magnetic latch. An advantage of the externally clocked latch is that the clock field dynamically reduces the switching threshold so that low current levels are sufficient to switch the slave device directly with the master output. The power required to generate the clock field in an external coil is not dissipated on chip.

We have demonstrated the operation of the latch and the dynamic threshold reduction using a discrete spin valve with a built-in easy-axis offset of 17 Oe. Shown in Fig. 3 is the probability of switching to the 1 state by a hard axis clock pulse as a function of the easy axis field. With a saturating hard axis pulse, the device is switched reliably with only 2 Oe field differential as opposed to the original 50 Oe switching field. The lower switching fields could, for example, be generated by 80 μA signal current in a 0.5 μm wide data line. Assuming a 2 ns current pulse is switched by a minimum length transistor in a 0.18 μm CMOS process, this will require at least 14 fJ per write, well under the power consumed by traditional CMOS registers reported in the next section.

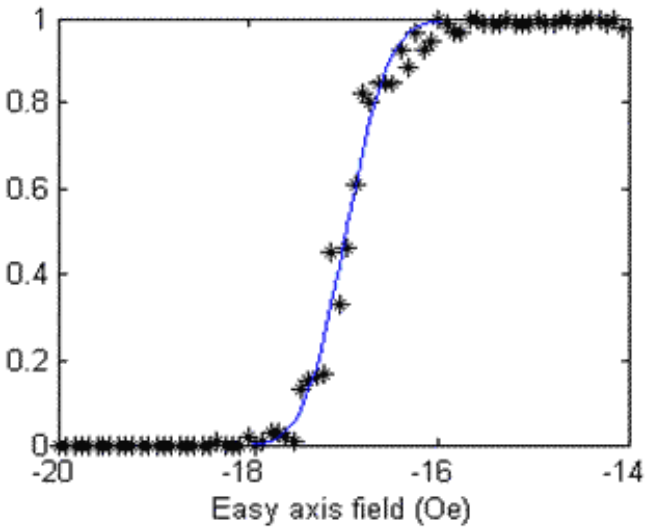

Figure 3: Measured switching of a spin valve in response to a hard axis clock field. The probability of switching to a 1 state is plotted against the easy axis field during the clock pulse.

4 Performance Benefits

4.1 Empirical Study of Hybrid CMOS-Magnetologic Designs

The goal of the empirical study is to assess the benefits that one might obtain from incorporating magnetologic master-slave flip-flops driven by a global external clock into a CMOS digital design. This approach has several potential benefits:

- elimination of the clock distribution network,
- reduction of on-die power consumption,
- reduction of chip area, and
- higher clock frequency due to elimination of clock skew.

In this empirical study, we experimentally assess the benefits of magnetologic in current CMOS semiconductor designs. We use a pair of digital designs that meet several criteria: 1) they are sufficiently large that their clock distribution network is substantial; 2) they use traditional synchronous design techniques; and 3) they operate using a single clock domain.

The first benchmark application is a Monte Carlo estimation of π (MC). It estimates π by generating a pair of uniformly distributed pseudo random numbers $(x, y), 0 \leq x, y < 1$ [6] and checking to see if the point defined by the pair falls within the first quadrant of a unit circle. The second benchmark application is a hardware priority queue (PQ). Records, comprised of a 32-bit key plus a 32-bit tag, are managed using a systolic array architecture that orders the keys using a pairwise compare-and-swap algorithm [7].

4.2 Methodology

For each of the above benchmarks, we perform a standard cell layout using traditional CMOS technology. We then use extracted information from the traditional layout to assess the impact of the use of magnetologic memory elements in a hybrid design that relies on CMOS standard cells for the combinational logic.

As part of the empirical study, specific choices were made with respect to tool set, standard cell library, and process technology. While the particular choices made are described below, in each case the ultimate determining factor was availability of the tool set, library, or process. In short, these choices were pragmatic.

We used the Cadence CAD tool flow to generate CMOS designs all the way to layout using the VTVT 0.18 μm standard cell library [8]. This library is frequently used for academic chip designs.

Once the layout is complete, the tool set provides area, power, and speed estimates for the resulting design, including not only totals but also quantities associated with portions of the design (e.g., power requirements for the clock distribution network). These values are used to estimate the performance gains achievable if the memory cells are replaced in the design by magnetologic master-slave flip-flops.

4.3 Results

Table 1 presents the properties of each benchmark layout. Both of the two benchmarks are area limited by wiring, so the percentage of total area consumed by the standard cells is reported as a fraction of the total area. All of the provided power estimates were generated using a statistical power model with a default activity level of 30%. The statistical model uses a probabilistic model to predict the power dissipation by assuming a default activity level (switching frequency) at the input to the combinational logic circuits.

Table 1: Properties of benchmark layouts

	Benchmark Design	
	MC	PQ
Total Area	75.1 mm^2	20.4 mm^2
Std. Cell Density	86%	83%
Total Power	2.7 W	0.84 W
Clock frequency	74 MHz	124 MHz
Clock period	13.5 ns	8.1 ns

To assess the benefits of using magnetologic to replace the the memory in the original CMOS design, we are interested in the impact of removing the clock distribution tree (since it is no longer required given a global external clock signal). Fig. 4 shows a decomposition of the power consumption into 3 components: combinational logic, registers, and clock drivers. This decomposition is provided for a range of activity levels. The fraction of power attributable to the clock drivers can potentially be eliminated in a hybrid CMOS-magnetologic circuit. This results in a power savings of between 25% and 40%.

Table 2 shows results for both area and timing. The fraction of the wiring area attributable to the clock distribution tree is estimated by wire length. Area savings of 4% to 8% are to be expected by elimination of the clock net. Timing benefits will be due to two factors, elimination of clock skew and reduced (wire) propagation delay due to reduced wiring congestion. We estimate only the first of these, with both absolute clock skew data provided as well as skew relative to the total clock period.

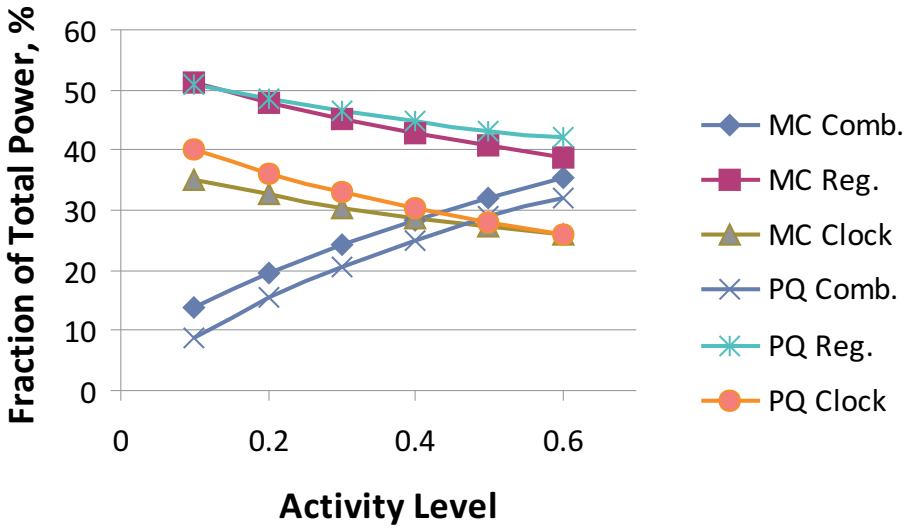

Figure 4: Power distribution results as a function of activity level.

5 Conclusions and Future Work

This paper has proposed the use of spin valve devices as the basic element for implementing registers in digital circuits. A master-slave flip-flop design is presented, which exploits a global magnetic field for clocking.

In assessing the viability and benefits of these ideas, a traditional CMOS layout of a pair of benchmark circuits is used to predict performance gains for the hybrid CMOS-magnetologic circuit in terms of power, area, and speed. For the benchmark circuits, we see power savings of 25% to 40% (depending on the activity level of the circuit), area savings of 4% to 8%, and speed improvements of approximately 3%. This does not include the potential area savings from converting all static CMOS latches into magnetic latches.

There are a number of items that need further investigation. We are currently in the process of fabricating a number of the basic elements using tunnel junction spin valves. This requires optimizing the switching thresholds and internal magnetic field offsets of the spin valve devices (including device variability), a technically difficult but not insurmountable design and fabrication challenge. In addition, the efficient generation of short input current pulses time synchronized with the external field is needed for high integration

Table 2: Area and Timing Results

	Benchmark Design	
	MC	PQ
Total Wiring Length	79 m	10 m
Clock Net Wiring	4.4%	7.5%
Clock Skew	342 ps	239 ps
Clock Skew %	2.5%	3.0%

levels. Current MRAMs only have the need to write to a minimum number of memory elements at a time. Use of magnetologic for general purpose registers will require power-efficient writing. Finally, we would like to investigate the use of spin-torque transfer switching as the write mechanism.

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