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Data Flow Design for a Gamma-Ray Telescope

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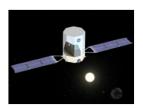
DATA FLOW DESIGN FOR A GAMMA-RAY TELESCOPE



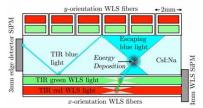
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Background

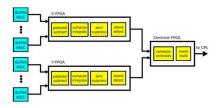
- The Advanced Particle-astrophysics telescope (APT) is a planned space telescope
- Detects gamma-ray bursts (GRB) and promptly communicate with other instruments for realtime follow-up observation
- FPGAs preprocess the raw data to be sent to the CPU



The telescope detects gamma-ray photons in space

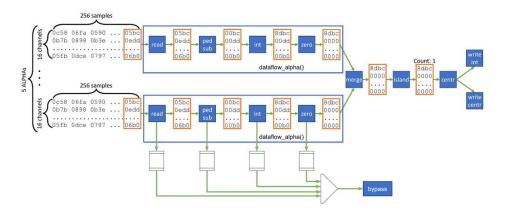


Photons enter the detector and light up fibers



Methods

- · Add a bypass channel to the existing data to handle debugging and pair production events
- Use C++ and High-Level Synthesis to develop the FPGA design



```
void dataflow_alpha(const vec_uinti6_16 * samples,
    hls::stream(Header> & header_stm_in, // contains all read-only information
    hls::stream(Header> & header_stm_out, // contains all read-only information
    hls::stream(vec_int32_16> zeroed_integrals[NUM_ALPHAS],
    hls::stream(vec_int32_16> rew_pair_data[NUM_ALPHAS],
    const uinta_t banks(NUM_ALPHAS],
    const uinta_t banks(NUM_ALPHAS),
    const uinta_t starting_sample_numbers[NUM_ALPHAS],
    const uinta_t alpha
    ) {
    *pragma HLS FUNCTION_INSTANTIATE variable=alpha
```

```
hls::stream
hls::stream
rec_uint16_16> packet_samples;
hls::stream
rec_uint32_16> pac_sub_results;
hls::stream
rec_uint32_16> integrals;
```

```
Header::Header(vec_uinti6_16 input_all_peds_in[NUM_ALPHAS][2*NUM_SAMPLES],
for (int i = 0; i < NUM_ALPHAS; ++i) {
    for(int j = 0; j < 2*NUM_SAMPLES; ++j) {
        for(int k = 0; k < 16; +k+) {
            input_all_peds[i][j][k] = input_all_peds_in[i][j][k];
        }
    }
    for(int j = 0; j < 2*NUM_INTEGRALS; ++j) {
        bounds[i][j] = bounds_in[i][j];
    }
    for(int j = 0; j < NUM_INTEGRALS; ++j) {
        zero_thresholds[i][j] = zero_thresholds_in[i][j];
    }
}</pre>
```

Accomplishments/Current Status

- Refactored the code to support stream-based inputs
- Built a bypass path to store a buffer of pedestal-subtracted data
- Changed metadata flow to move with main data packets

Future Work

- Creating additional bypass pathways and control logic for selecting a data stream
- Analyzing additional buffering requirements on overall FPGA
- Update packet definitions across the entire pipeline to be compatible with bypass
- Enable the FPGA-to-FPGA data communications, including accommodating the bypass path
- Enable the FPGA-to-network-to-embedded processor communications, also accommodating the bypass path

Lessons Learned

- Usage of high-level synthesis for FPGA layout
- Data flow and computation architecture (parallelism through pipelining)
- Advanced stream management in C++

Acknowledgements

Thank you to Roger Chamberlain, Marion Sudvarg and James Buckley

References

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