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Toward Devices for Exploring \mathcal{PT} -symmetry in Electronic Transport of Graphene

Michael Carovillano

(Dated: March 17, 2019)

Abstract

Parity-time symmetry, or \mathcal{PT} -symmetry is the principle that in quantum mechanics a non-Hermitian Hamiltonian is capable of returning real eigenstates and real spectra.¹ Recent research has demonstrated real world observation of \mathcal{PT} -symmetry in electronics and optics^{2,3,4}. We aim to expand the regime of observed \mathcal{PT} -symmetry through measurement of the electronic transport of graphene devices. Drawing from analogous experiments, we plan to use balanced ohmic resistance acting as both loss and relative gain to induce the required unbroken \mathcal{PT} -symmetry regime. This paper analyzes techniques used in fabrication of such devices as well as the basis of the design and measuring methodology, with aims of observing \mathcal{PT} -symmetry in diffusive electronic transport of graphene, with plans for expansion into ballistic transport.

I. INTRODUCTION

\mathcal{PT} -symmetry is a means of extending the Hamiltonian describing a quantum system into the complex domain through use of non-hermitian Hamiltonians. The Hamiltonian describing a quantum system is typically thought of as being Hermitian, that is, the complex conjugate of the function is equal to the conjugate transpose; however, this has been proven to not be a necessary constriction in the case of the function retaining symmetry in both space-time reflection (parity) and time simultaneously⁵. The result of this shows that a complex, non-hermitian function can have real eigen-energies.

The implications of these new Hamiltonians are far reaching, resulting in numerous papers being published in the field of \mathcal{PT} -symmetry^{1,6}. The real world expression of these \mathcal{PT} -symmetric functions have been classically observed, such as in optics^{3,7} and electronics². Our project creates an analogous system to the optical observation using the electronic transport of charge carriers in graphene with aims aims of observing the effects of \mathcal{PT} -symmetry.

\mathcal{PT} -symmetry has been observed in systems utilizing equivalent gain and loss^{2,3}. However, some forms of \mathcal{PT} -symmetric systems cannot exist with gain and loss while retaining good signal to noise ratio⁸. In an attempt to minimize noise, our experiment uses relative gain, with both channels experiencing loss. This passive \mathcal{PT} -symmetry system will allow us to avoid thermal and other introduced ambient noise from adding gain to such a system.

To introduce the loss into the system for diffusive electronic transport in graphene, a top gate will be fabricated on the device with a dielectric consisting of hexagonal boron nitride (h-BN) separating the gate from the graphene. This top gate will allow modulation in the conductivity of the graphene by altering the charge carrier density of the system using a voltage differential. By sweeping the voltage over a wide range, the conductivity can be tuned, thus allowing for effective loss in the system. By covering exactly half of the device with this gate, the graphene is effectively split into two regions - one strongly coupled to the effects of the top gate, and the other side left largely unaffected by the voltage changes in the top gate - thus allowing the conductivity to be tuned in each region independently. By placing the gate over the entire half of the device and not leaving areas uncovered, we reduce the chance of anomalous electron paths or rapid changes in the mean free path except at the desired boundary region. In order to further extend the range of charge carrier density change, the entire device is built on a wafer of silicon with a thin layer of silicon dioxide

(SiO₂) approximately 300 nm thick insulating the graphene from the substrate. The Si substrate acts as a global back gate, affecting the charge carrier density of both regions of the device. In both gate cases, the change in charge carrier density alters the Joule heating ohmic resistance and thus allows us to tune the loss of the system to the \mathcal{PT} -symmetric regime of 50% (relative) gain and 50% loss.

II. DEVICE FABRICATION

The fabrication of these \mathcal{PT} -symmetry devices draws from and develops common techniques used in the manufacture of micron scale 2-D electronic devices^{9,10}. The total time and number of steps required to make a device changes on a case by case basis, with some steps requiring long intervals for pulling vacuum or allowing for chemical processes to occur. In certain steps, undesired results can be undone and the process repeated. This makes it impossible to put a specific number of hours to the general process. The device used as a case study in this paper was fabricated over the course of multiple weeks in collaboration with members of the Henriksen Lab Group. This paper will analyze and show developments in the fabrication process through this case study, demonstrating researched techniques and providing insight for future endeavors.

A. Exfoliation and Preparation of Materials

Graphene and hexagonal boron nitride are prepared in the lab using the “Scotch tape method” of material exfoliation pioneered by Geim and Novoselov^{9,11,12}. Different types of tape have been tested to determine which variant maximizes yield of usable flakes of desired thickness and quality while minimizing the amount of residue and other contaminants, with Scotch matte Magic Tape yielding the best consistent results for our group. Even within a specific tape product, there is variability attributed to storage and transport conditions, thus making the sourcing important to ensure that the tape has not been exposed to extreme temperatures, which increase tape residue. Once exfoliated, the materials are then deposited onto a diced silicon dioxide wafer substrate for optical identification and analysis. Visual color analysis is used to determine approximate thickness of h-BN flakes while high contrast imaging is used to identify impurities or imperfections in the samples to select suitable

pieces to serve as a thin dielectric between the graphene and top gate. High quality pieces of sufficient size and thickness are cataloged for future pickup and drop off onto the graphene sample, as well as use in other devices. Graphene is also identified by image analysis and left on the SiO_2 wafer once identified and cataloged. Typically, the graphene used in device making is picked up and deposited onto a prefabricated wafer. Through testing various methods, it was determined that leaving the graphene sample on the wafer it was exfoliated onto and fabricating the device on the initial wafer reduced number of fabrication steps and thus improved rates of device survival. Thus, for these \mathcal{PT} -symmetry devices, all fabrication takes place on the initial Si wafer with a SiO_2 surface.

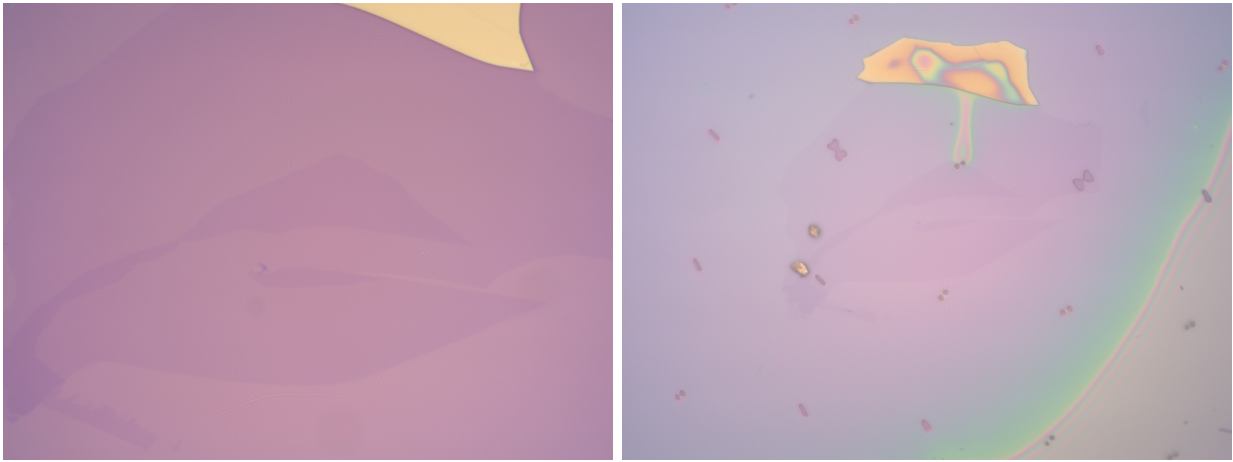


FIG. 1.

(Left) A sheet of graphene with a strip of bi-layer graphite running through the center. A thick piece of graphite can be seen in orange at the top. (Right) PMMA spun onto the surface of the wafer with alignment marks written into the surface with e-beam lithography.

While this is a useful substrate for exfoliation and some diffusive observations, the disordered nature of the substrate interferes with the intrinsic properties of the device being measured^{13,14,15}. The use of boron nitride as an encapsulating material has been demonstrated to significantly increase the quality of graphene and other atomically thin devices^{16,17}. This increased mobility is attributed to h-BN having an atomically smooth surface with minimal irregularities that could cause interference in electron path, as well as a similar lattice constant between h-BN and graphene¹⁸. This makes h-BN an ideal dielectric in most cases, while also being excellent as an encapsulating material for use in ballistic transport. For the case of diffusive transport, a SiO_2 substrate with a flake of h-BN is sufficient, with mobility

improving with a more uniform contact surface¹⁹.

Over the course of time spent in lab, different variables such as applied pressure, tools and surfaces used, amount of time spent on each step, and various other techniques were altered to see how various methods of exfoliating affected yield of usable flakes. From early iterations of the exfoliation process, normal yields were approximately two to three usable flakes of h-BN per diced chip of silicon wafer. By investigating said variables and prepping the materials and wafer using a chemical wash and percussive cleaning, yields of over twenty-five usable flakes of h-BN per diced wafer are now possible. The quality and size of flakes has also improved, allowing for cleaner devices of a higher quality and electron mobility.

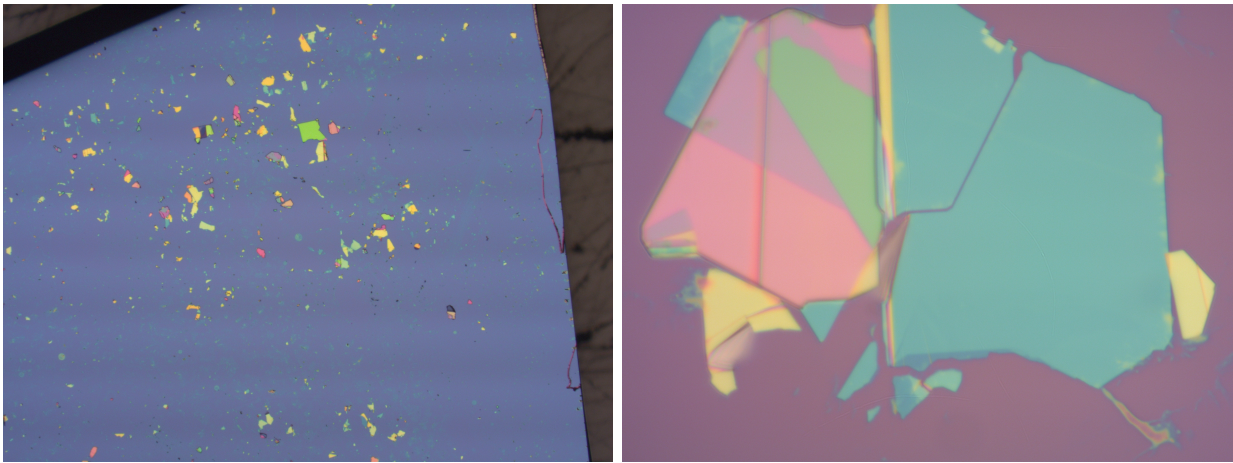


FIG. 2.

(Left) A SiO_2 wafer with exfoliated h-BN deposited on the surface of varying thicknesses.
(Right) An sample of h-BN demonstrating how the thickness of the material affects the color. Usable pieces tend to be from the lightest blue to a blue-green color, as seen in the large surface area of the shown flake. The color goes through the wavelengths of the visual spectrum, with blue being the thinnest and red being thicker. Colors repeat after a certain thickness, requiring visual checks for extra layers.

B. Lithography and Evaporation

Once a suitable piece of graphene has been identified, designing the wiring of the system may begin. The writing of wires onto the surface of the device is a multi-stepped process that requires multiple iterations to ensure quality of the device and allow for insulation between layers. Certain steps can be undone and repeated if the outcome is unfavorable, as mentioned in II. However, other steps such as evaporation and liftoff are irreversible, leaving

the user to work with whatever the result may be. In the case study of this paper, during lithography, two wires were shorted to one another in the alignment process of the e-beam. This ultimately did not affect the performance of the device, however, since it was designed with redundant contacts in each region.

1. PMMA

PMMA (polymethyl methacrylate) is used as a high resolution positive resist for direct electron beam (e-beam) lithography. The wafer with the graphene sample on it is pre-baked on a hot plate at 180°C for 5 minutes, then secured to the spin coater using a vacuum chuck. PMMA with molecular weight of 495k and 950k are used in layers to create a thin film for the lithography. The 495PMMA is deposited directly onto the surface, then spun on the spin coater, ramping up to a relatively slow speed of around 2000 RPM. This slower speed allows for a thicker layer of 495PMMA as a base, evenly covering the graphene sample. The hot plate bake is then repeated and the wafer is secured on the spin coater again. 950PMMA is then directly deposited on the surface and spun, ramping up to around 4000 RPM to create a thinner layer. The bake is then repeated one final time. The higher molecular weight equates to a greater contrast between the exposed and unexposed regions of the film due to the greater number of bonds in the higher molecular weight polymer. The electron beam breaks the bonds in the polymer without removing it. A developing solution is then used to wash away the PMMA with broken bonds, leaving the polymer that was not written by the e-beam. An undercut is developed due to the 495PMMA below the 950PMMA having fewer bonds to break. The e-beam writes with a constant energy through the PMMA to the wafer surface below. The energy cost is thus greater to go through the 950PMMA. Additionally, when the e-beam reaches the SiO₂ substrate, there is significant backscattering into the 495PMMA, further developing an undercut. This undercut is used to aid in the sheering of the evaporated Cr/Au contacts to ensure clean breaks in the liftoff process. An undercut can also be developed using only 950PMMA and backscattering, however the undercut will be reduced due to the higher molecular weight of the polymer²⁰.

2. *Alignment Marks*

In order to provide to properly align the SEM and account for image distortion from the microscope, alignment marks are written on the wafer in the PMMA. A pre-designed, unique grid pattern of simple geometric shapes with $50\mu\text{m}$ spacing is used to determine the exact location on the grid from any two reference points.

To add this pattern to our PMMA coated wafer, it is uploaded to the SEM. The SEM field of view is centered over the desired flake and the pattern is written using NPGS (Nanometer Pattern Generation System). After chemical development in either IPA, IPA:DI water, or IPA:MIBK, the alignment mark pattern is optically examined for proper positioning over the graphene flake.

3. *Writing the Wires*

After the alignment marks are written, they are used to design a pattern of wires and bond pads for electrical contact to the graphene flake. Optical microscope images are imported into the alignment mark design so exact pattern alignment can be achieved. The contact wires to the graphene are designed with fine leads contacting the graphene that break out to coarse leads that terminate in large contact pads that can be more easily wire bonded to. Contacts are written using NPGS software and designed in DesignCAD software.

It is crucially important to the survival of the device that once wires are written, the utmost care must be taken to ensure that when handling the device, the user is always properly grounded. **A simple static discharge from a user into the device can cause sufficient damage to render the device unusable.**

4. *Evaporation of Chromium/Gold Contacts*

Once e-beam lithography has opened up a window on the device by cutting through the polymer to the wafer surface below as show in Fig 3, the metal contacts are then deposited onto the device through chemical vapor deposition in a thermal evaporator. Both chromium and gold are evaporated and deposited onto the surface using a vacuum evaporator. Chromium is deposited first as it adheres to the SiO_2 surface better than Au and binds well to gold as well. Titanium can also be used as a sort of “sticky” layer for the gold to

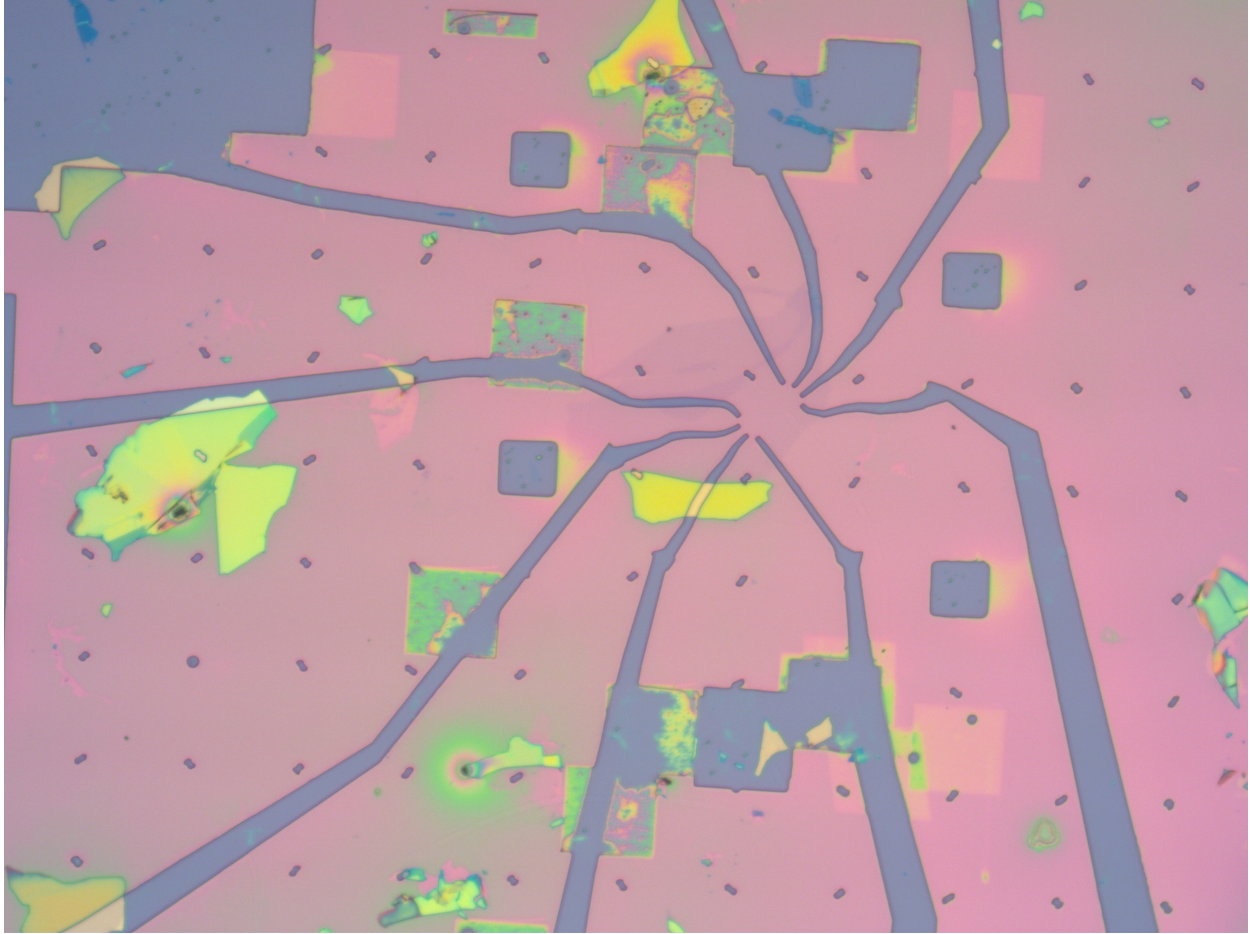


FIG. 3.

E-beam lithography of layered 495PMMA and 950PMMA. Alignment marks are seen spaced $50\mu\text{m}$ apart, with the square windows used to test alignment and exposure before writing the pattern.

bind to, however Cr is preferred for its ease of use. The gold deposition is then carried out, likewise covering the entire surface of the PMMA over the device. Where the lithography has opened windows to the substrate, the Cr - and thus Au - adheres to the surface, creating a slight indentation as the metal fills the volume of the cut. This

5. *Liftoff*

After evaporation, the PMMA resist film is removed using acetone at 50°C as a resist stripper. The Cr/Au deposited on the PMMA floats off the device as the PMMA substrate dissolves, sheering off from the metal deposited directly onto the SiO_2 surface and graphene, leaving behind clean contacts with sub-micron precision. The wafer is typically left in the

acetone for at least an hour to ensure thorough dissolving of the PMMA. In order to remove all metal not deposited directly onto the surface of the wafer, turbulence can be introduced into the acetone with a pipette, with liftoff being observed under an optical microscope to ensure complete removal. In extreme circumstances where residual gold is not lifting off, sonication can be used for extremely brief amounts of time (less than 1 second). This method is typically used as a last resort due to its aggressive nature and tendency to cause destruction of metal bonded to the graphene or substrate surface. Excess gold is acceptable so long as it is not shorting crucial contacts to others that would restrict the usage of the device.

C. Etching

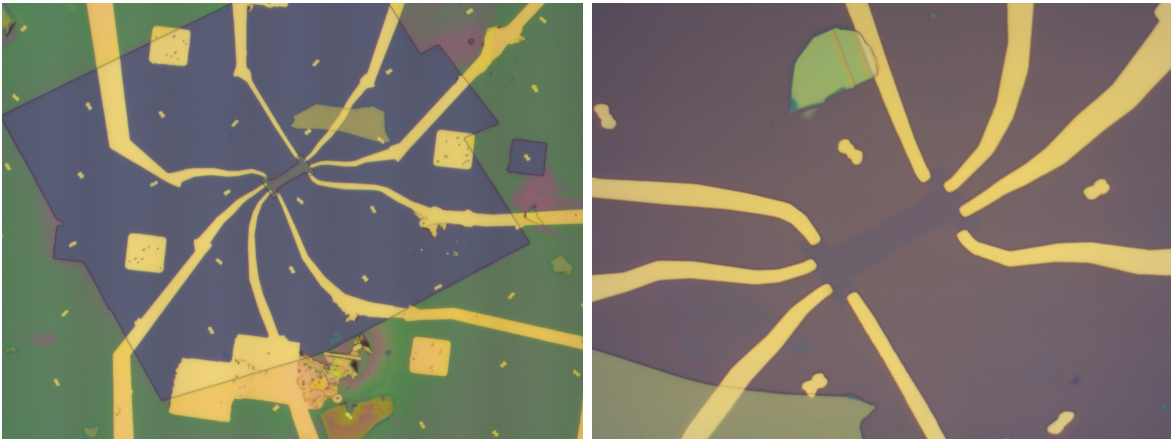


FIG. 4.

(Left) Lead window opened using lithography to create a negative image for etching away excess graphene. (Right) Graphene etched into desired I-beam shape.

With the wires written and in contact with the graphene, the sample is now etched into the desired shape. PMMA is once again spun onto the chip in the same manner as detailed in [IIB 1](#), but this time using multiple layers of 950PMMA without 495PMMA to reduce the undercut during lithography. Two overlapping polygons are then drawn in DesignCAD with the negative space between them forming the desired shape of the graphene sample. The area within each of the polygons will be written away during the lithography, leaving a protective etch mask over the sample. The area cut out to be etched should be large enough

to cut away all excess material that could potentially short contacts as well. The sample is then loaded into a vacuum chamber and exposed to ion plasma - $O_2:Ar$ in the case of graphene on oxide. The plasma etches all surfaces exposed to it, however because of the thickness of the PMMA, the excess graphene is etched away before the mask, allowing for precise shaping of samples.

D. Stacking of Materials

With all contacts written to the graphene and the device cleaned, a piece of h-BN is now placed on top to serve as the dielectric of the top gate. The h-BN is deposited after the contacts have been etched rather than before to prevent the contacts from shorting to one another once the gate is evaporated on. Usable h-BN flakes are identified using the methodology outlined in [II A](#). Once a usable piece is identified, the flake is picked up using a glass slide with a polydimethylsiloxane (PDMS) stamp a few millimeters square placed on the surface. The PDMS stamp is taped down uniformly to create a raised topography on the slide. A piece of polypropylene carbonate (PPC) is then placed on top of the stamp to act as the adhesive surface used to pick up the flake. The PDMS stamp has a convex topography, creating a single controllable touchdown point for the PPC slide. The slide is touched down next to the desired piece and heated so that the PPC slowly contacts the entire piece due to thermal expansion. Once the piece is covered, the van der Waals interactions allow the flake to be lifted off the surface of the wafer and stick to the PPC. The flake is then aligned over the device with the cleanest area of h-BN covering the graphene and slowly lowered to create a “stack.” Once contact has been made, thermal expansion is once again used to slowly deposit the flake over the device to minimize trapped pockets of air, folds in the material, or other imperfections. The temperature is continuously increased while slowly lifting off to melt the PPC onto the device, cleanly depositing the flake.

E. Writing the Top Gate

With the h-BN dielectric placed on the surface, the device is now cleaned in acetone to wash away the melted PPC residue. The graphene is now effectively protected beneath the uniform surface of the h-BN as show in [Fig 6](#). The same procedure as outlined in [II B 3](#) is

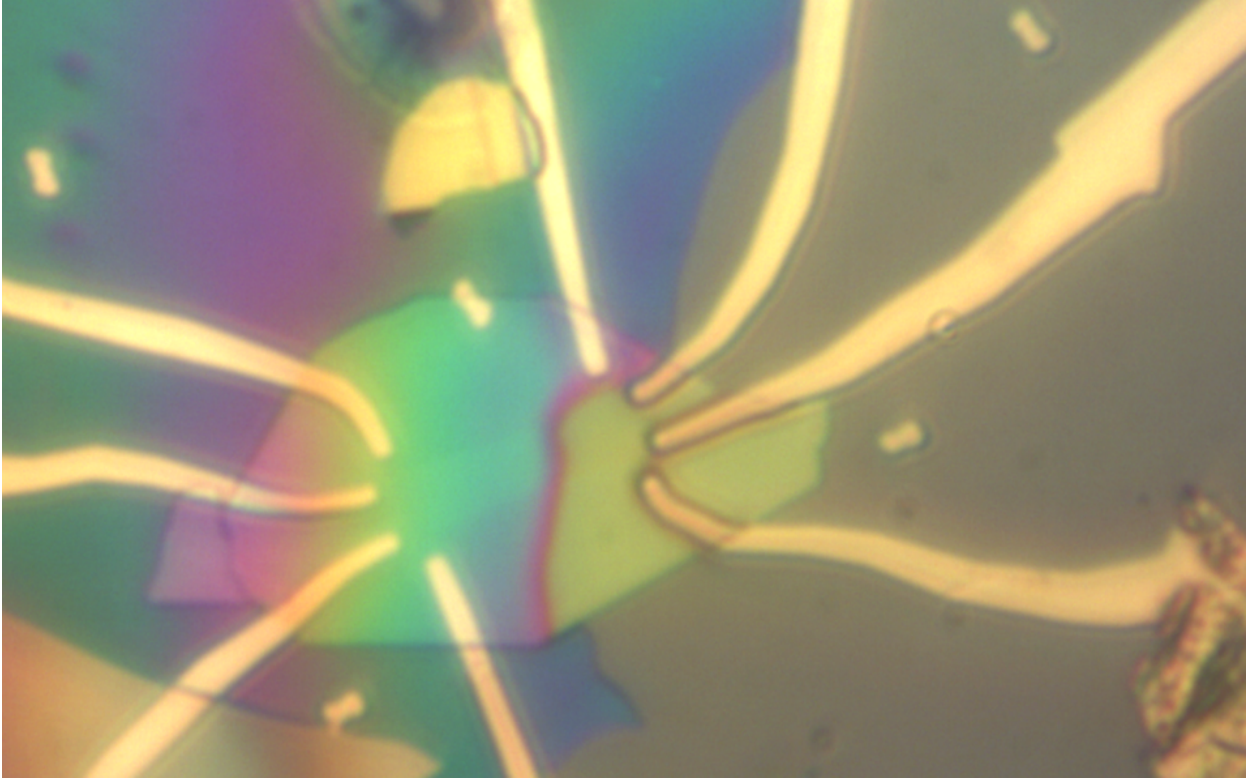


FIG. 5.

H-BN being dropped onto the surface of the device. The darker brown color on the right denotes contact of the PPC with the surface. The rainbow color is due to refraction through the PPC as it is contorted from the contact with the surface. Thermal expansion causes the contact front to slowly press down the entire flake evenly onto the device.

used to create the top gate using the NPGS and DesignCAD software. The e-beam writes through the PMMA to the h-BN surface below, but does not write through the surface as the etch rate of h-BN is orders of magnitude slower than that of the polymers. The development solution washes away the exposed PMMA leaving precise windows which will be used for Cr/Au deposition. The shape of the top gate is a simple plate capacitor to alter the charge carrier density as described in I. The shape of the gate reduces edge effects by extending past the edge of the graphene in all directions except the middle line separating the two regions. This is achieved by selecting a piece of h-BN that extends far enough to provide a clean level surface that the gate can be deposited on while serving as a dielectric.

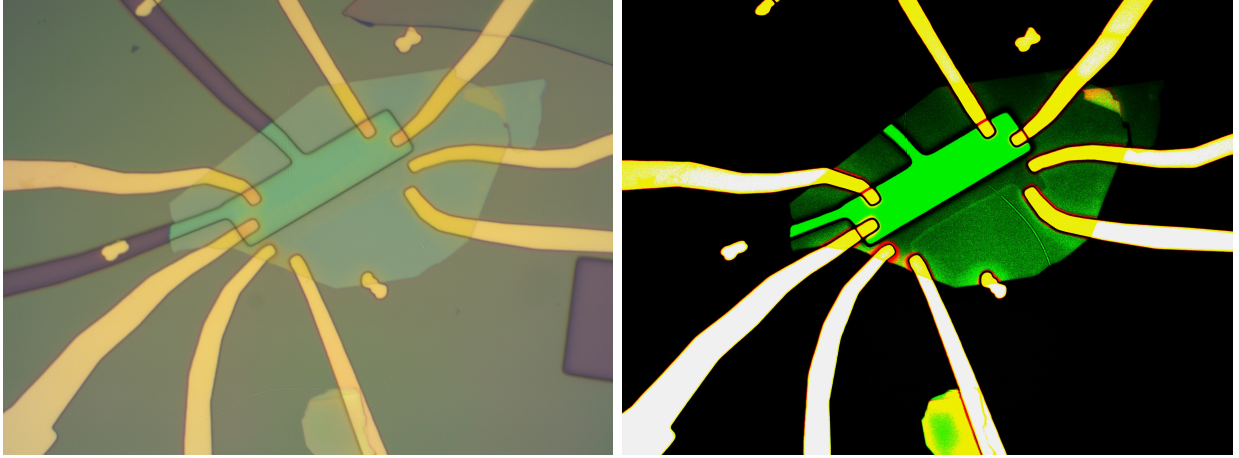


FIG. 6.

(Left) Top gate lithography cut through the PMMA to the substrate below, exposing the SiO₂ and h-BN surfaces for evaporation. (Right) A high contrast image showing the shape of the graphene beneath the h-BN.

F. Preparing for Measurement

These \mathcal{PT} -symmetry devices are a few hundred microns (μm) long in total, including alignment marks and ample space around the actual device. This scale requires an interface between the leads on the device and the contact pads inside the measurement system. Measurements are taken in either a BlueFors dilution refrigerator or a Physical Properties Measurement System (PPMS), which both use different interfaces to connect with the device. In order to standardize the interface such that \mathcal{PT} -symmetric devices can be measured in both systems, universal sample mounts have been designed and produced as discussed in [II F 1](#).

1. Universal Sample Stage Plates

Previous sample mounts have run into compatibility problems with different kinds of devices with varying contacts, as well as different measuring systems. Thus, a new universal sample stage plate was designed and fabricated using the LPKF ProMat circuit board plotter and LPKF Contac electroplating device to allow for the streamlining of device measurement.

Each device is now given its own dedicated sample plate that it is wire bonded to. The new universal sample stage plates are capable of accommodating every kind of device currently made in the Henriksen Lab Group, including but not limited to: IR, adatom, and EMR

devices, while also being compatible with every measuring system we employ. Each copper contact pad contains a through plated via hole. These holes are drilled into the contact pads of the device on one side and through to the corresponding contact pad on the reverse side. The channel created by the drilling is then electroplated with copper to create electrical contact to the symmetric contact pad on the reverse side. This allows for the device on the chip to be wire bonded to the sanded copper pads, and then for the entire sample plate to make contact with the measurement interface by being placed on top of fuzz buttons - strands of gold-plated beryllium copper wire bunched up into a ball of material allowing for expansion to ensure good contact. This streamlined process allows for easier cataloging of devices mounted to plates, quicker measurements, and overall greater convenience in the gathering of data.

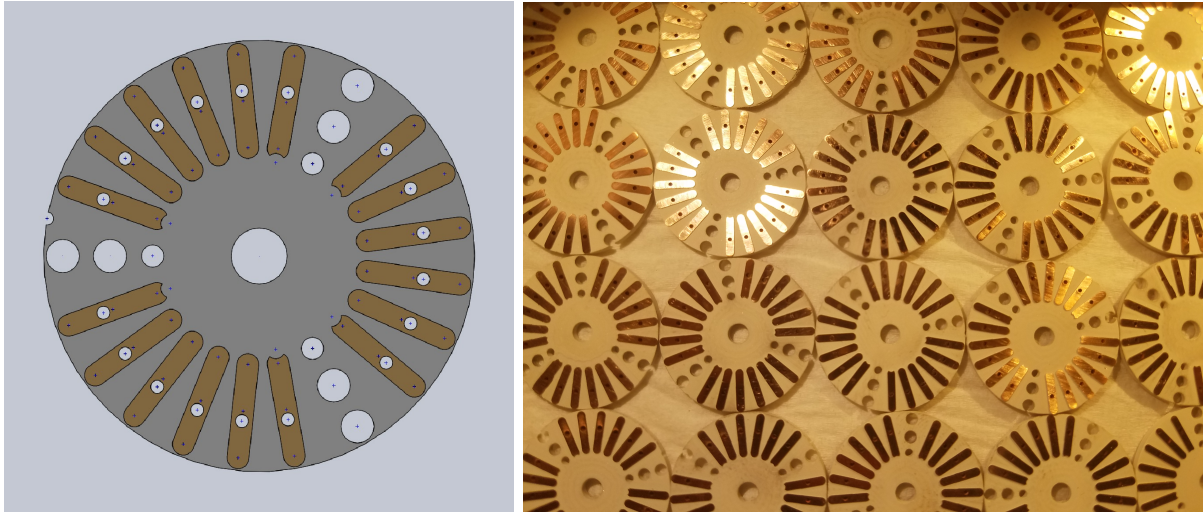


FIG. 7.

(Left) A SolidWorks design of the new universal sample mount system mk3, which was exported and used as the design cut by the LPKF Promat. (Right) Finished fabricated sample plates with copper pads sanded to allow for optimal wire bonding.

2. *Mounting and Wire Bonding*

Once fabrication has been completed, the device wafer is further diced down to fit within the center region of the universal sample stage plate. A razor blade can be carefully placed on the wafer to shield the device from dust created during the dicing, however, the h-BN protects the graphene sample sufficiently well. Once cut down to size, the wafer containing

the device is then attached to the sample plate using one of several methods. Physical clamps, double sided kapton tape, rubber cement, and vacuum grease have all been used to secure the sample to the plate. Crucially, all of these methods perform well repeatable at cryogenic temperatures. In this case study, vacuum grease was used to secure the wafer.

Once on the plate, a West Bond manual wire bonder equipped with 1 mil (0.001 inch) gold wire is used to bond the contact pads on the device to the contact pads on the plate. The device uses ultrasound to bond wires to the Cr/Au contact pads. The entire process is done manually through a binocular microscope. Gold wire is used as it bonds well to both the Cr/Au pads on the device and the sanded copper pads on the plate, however other metals such as aluminum can also be used. The user is grounded out during this entire process to ensure no static discharge can go through the device and damage it.

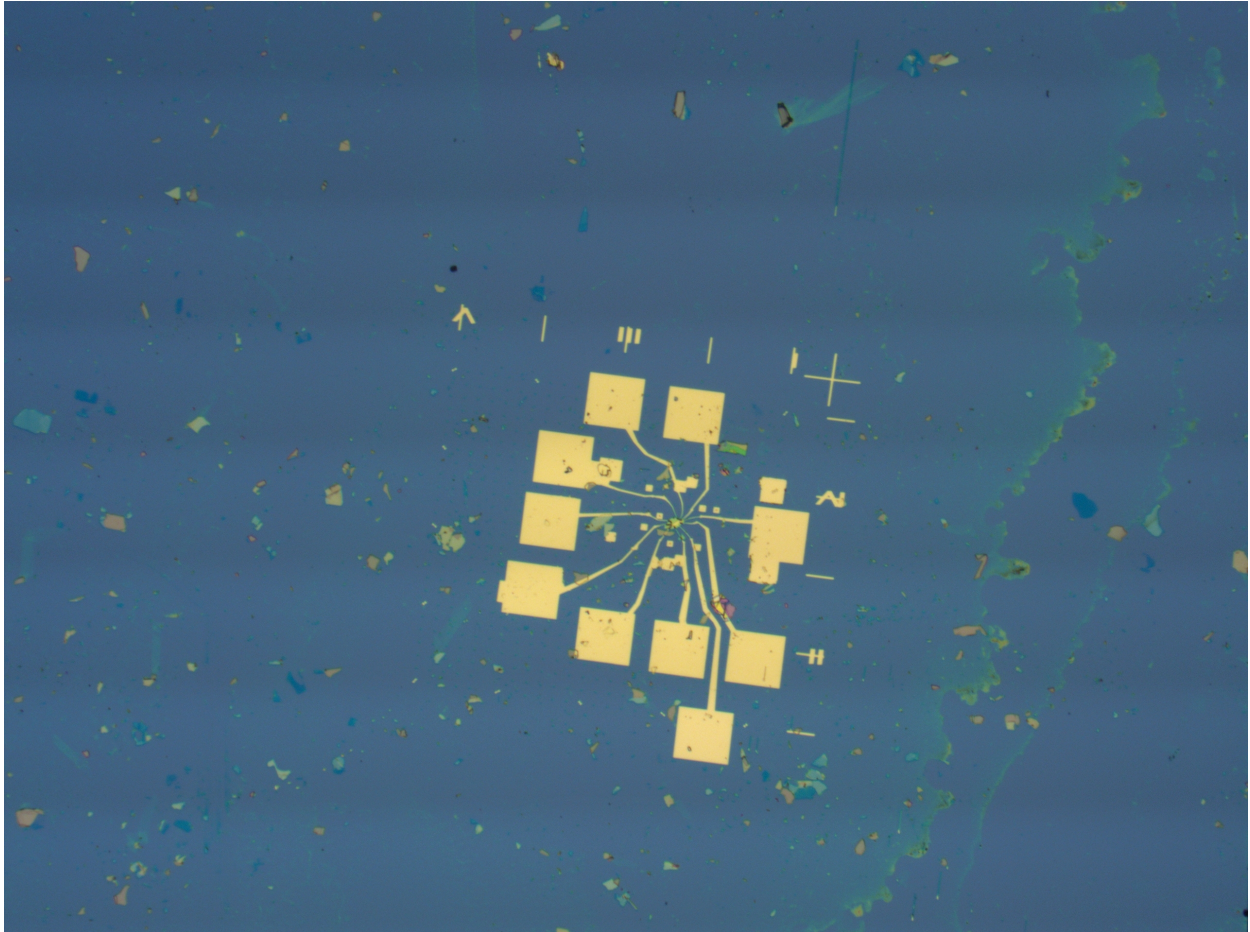


FIG. 8.

A completed device with rough contact pads breaking out from the contacts to graphene sample and the top gate written over the h-BN dielectric. These large squares are the contact points used for wire bonding to the sample plate.

III. MEASUREMENT

The PPMS system will be used to measure the electronic transport in these devices. Measurements will be taken at around 3 Kelvin and extreme vacuum pressure to reduce phonons and other interference to a minimum. In order to more accurately source voltage and protect the devices from large current flow, a 100:1 voltage divider is used on both the top gate and the global back gate.

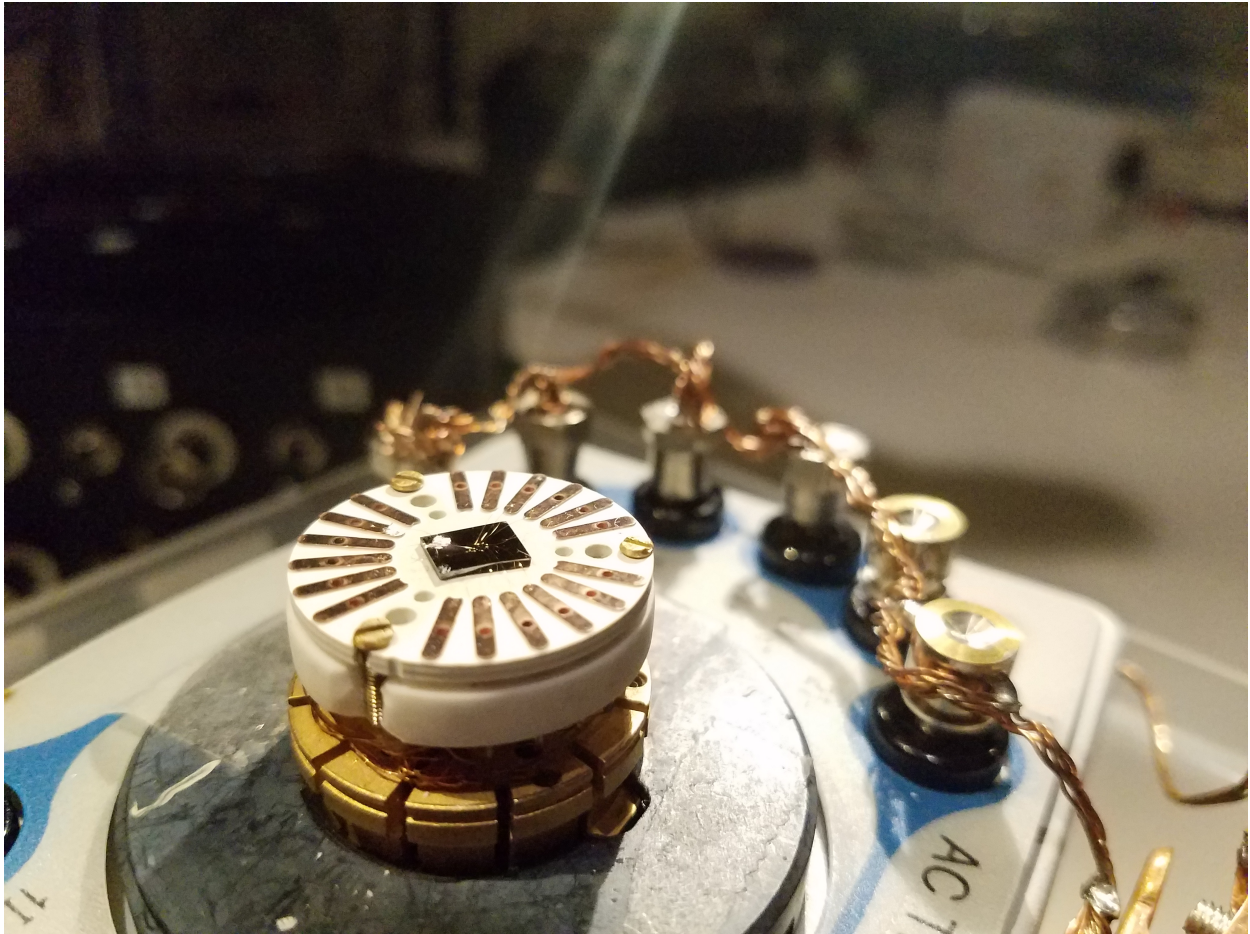


FIG. 9.

A completed device mounted to the sample chuck used to load samples into the PPMS. The device is always transported while connected to a carrier that ensures all contacts are grounded to prevent potential damage to the device.

A custom-written program will be used to automatically perform a two gate voltage sweep of the device. The back gate will have its voltage incrementally changed, with the top gate performing a full range sweep at each increment. By taking continuous measurements at each increment, a graph of the voltage of the top gate (V_t) on the y-axis, and the voltage of

the back gate (V_b) on the x-axis can be created.

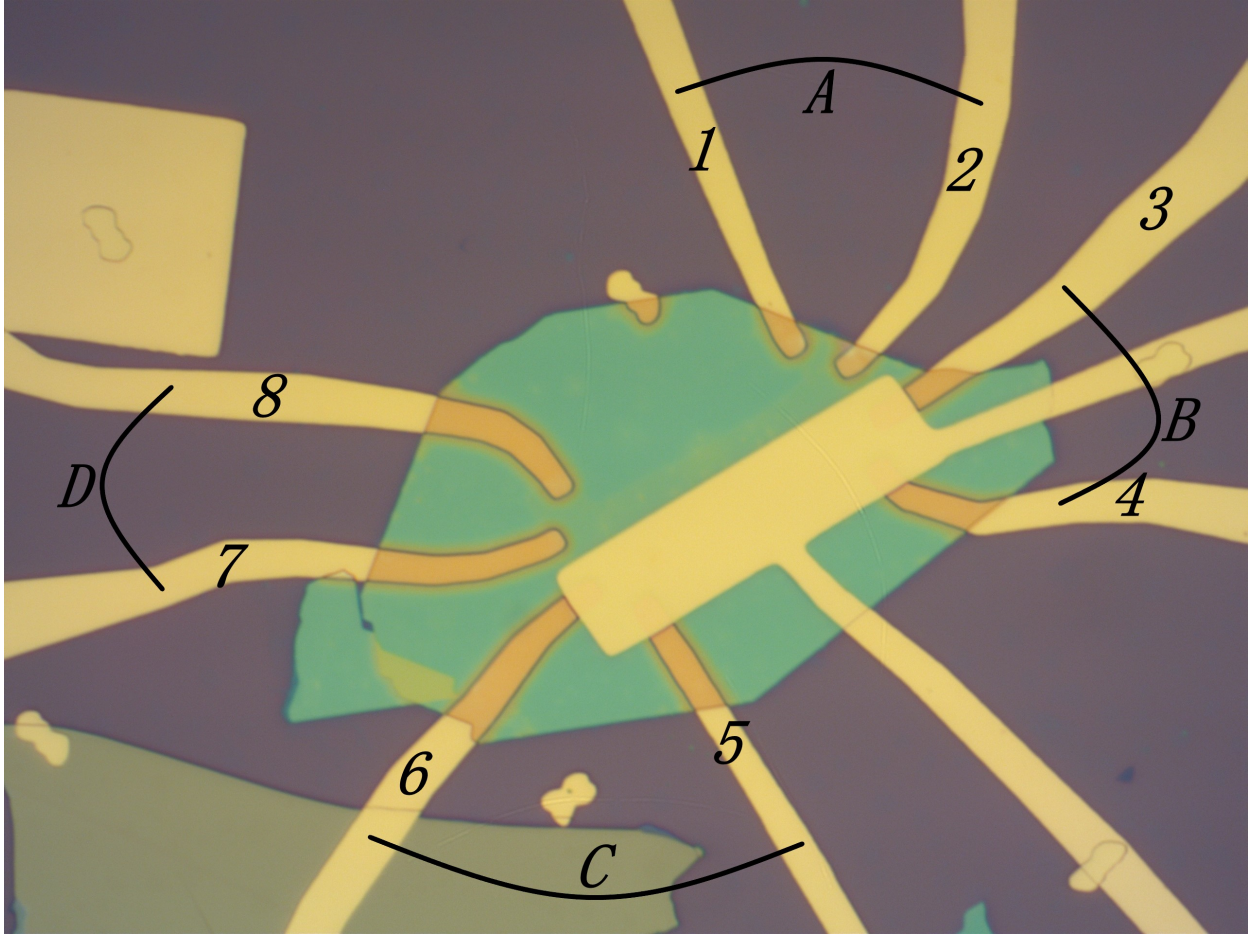


FIG. 10.

A completed device with contacts to the I-beam shaped graphene (shown in Fig 4 and 6) labelled and grouped. Group A (contacts 1 & 2) and group D (8 & 7) are connected to the graphene in the ungated region while group B (3 & 4) and group C (5 & 6) are in the gated region.

Due to symmetry of the device, the choice of sourcing and measuring groups can be mirrored, with groups A and B acting as either current source or measuring contacts, as shown in Fig 10. In this situation, let's assume current is sourced from contacts in groups D and C and measured from groups A and B. The grouping of contacts is a redundancy to ensure good contacts are available in all regions. Current will be sourced from D alone, then C alone, then D and C simultaneously. Likewise current can be measured from both groups A and B simultaneously or independently. The resulting current coming out of A (I_A) can be graphed in the color axis of the previously mentioned graph of V_t vs V_b . Likewise, I_B and,

most importantly, the difference of currents, I_{A-B} , can be plotted. This plot should show a discrete point of broken vs unbroken \mathcal{PT} -symmetry regimes, with an observable change in current at the boundary region.

Four point measurements can also be taken by applying a voltage into contact 7 and measuring the current via lockin-preamp to ground at 2 while simultaneously measuring the voltage across contacts 8 and 1. This gives a standard four point Rxx measurement. This measurement can be repeated, such as sourcing voltage at 8, measuring current at 1, and measuring voltage across 7 and two, or reverse the process with source at 5, current measurement at 4, and voltage measurement across 6 and 3.

IV. DISCUSSION

This fabrication process and described measurement technique will be used to make and measure more devices for the diffusive regime of electronic transport in graphene. The device used as a case study in this paper went through the entire fabrication process seemingly without issues. When measured in the PPMS, however, all contacts read a resistance of greater than 50 M Ω . After a thorough investigation through every part of the fabrication process, it was determined that a static discharge from a user at some point went through the device and damaged all contacts. This is unfortunately a common occurrence in 2-D and micron scale device fabrication. Steps have thus been taken to allow for the simultaneous fabrication of multiple devices, increasing total output to allow for a greater number of measurable devices. Several new devices with the same basic design are currently being fabricated with hopes of measurements of electronic transport in the coming weeks.

V. FUTURE DEVELOPMENTS

Measurements can also be made in the ballistic regime of electronic transport. Some alterations to the device design will be made to optimize chances of observation of \mathcal{PT} -symmetry effects. For example, ohmic resistance cannot be used as the source of loss in the ballistic case of electronic transport. The loss of the system will be introduced using grounded contacts on one side of the graphene device that let electrons exit the system when the channel is open, thus allowing for the amount of loss to be controlled with how many

channels on the loss side are opened. The mean free path in this case will still be ballistic motion even with a gate, however a boundary region will be created where electrons will need to change energy to pass the edge of the gate; this effect is heightened if one side is p-doped and the other side is n-doped, thus creating an electric field at the boundary that discourages electrons from passing through.

In the case of elastic ballistic electronic transport, changing the charge carrier density changes the Fermi energy of the system, thus affecting the conductivity. By altering the energy between the two regions, electrons are forced to lose or gain energy to cross the barrier so there is resistance to switching between regions of the device. This is analogous to evanescent coupling in the optical wave guides in experiments showing \mathcal{PT} -symmetry in optics. These methods are adapted from the experimental set up seen in the the observation of \mathcal{PT} -symmetry in optical devices³. Our aim is to create an analogous experiment that will function in the electronic transport of graphene devices.

The fabrication of the ballistic regime \mathcal{PT} -symmetry devices will follow a similar process as the diffusive transport with a few key exceptions. Along with the aforementioned grounded side contacts, the device will also be encapsulated in h-BN rather than resting on a comparatively “dirty” substrate of silicon dioxide that will cause diffusive transport. The “clean” h-BN encapsulated flip stack will allow for ballistic transport of electrons. Rather than completely depositing the h-BN onto the surface of the device as described in IID, the h-BN will be used to pick up the graphene and flip the whole stack over so that the h-BN is the substrate. Since the whole stack has been picked up, a prefabricated wafer with clean contact pads and regular symmetry can be used to cut down on total number of steps needed and reduce total number of sources of error. The contacts are then fabricated in the same method and the top h-BN is deposited, creating an encapsulated device with higher mobility. This will allow for research in multiple regimes of electronic transport, furthering the scope of study into \mathcal{PT} -symmetry observed in graphene devices.

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